www.ijaceeonline.com ISSN: 2456 - 3935

International Journal of Advances in Computer and Electronics Engineering
Volume 3, Issue 5, May 2018, pp. 9–13

Silicon Wafer Specifications and Its Selection Criteria

Kamaljeet Singh
Sci/Engr, ISRO Satellite Center
Email: kamaljs@isac.gov.in

Ayyappankavu Venkateswaran Nirmal
Group Director, ISRO Satellite Center
Email: avnirmal@isac.gov.in

Abstract: *This article details the specifications of silicon wafers employed in varied applications as wafers for sensor requirement can be different from integrated circuits. Also stringent specifications like low leakage, latch-up immunity require wafers having different specs than standard wafer. Silicon wafers such as SOI, epitaxial, high resistivity differ in parameters compared to standard wafer. The wafer parameters are different for each class of wafer and specifications of the same to be chosen carefully as electrical performance is directly proportional to it. Apart from orientation, thickness, size various other parameters are defined in generating the wafer parameters and this article details the specs associated with above wafers.*

Keyword: *Silicon; wafer; parameters; type*

1. INTRODUCTION

Demands for integrated circuits are on rise and continual requirement of having the chip with enhance performance and low cost is driving this push. This necessitates to optimize the performance of the existing circuit for which wafer plays an important role. Trends in VLSI technology leads to continuous shrinkage of transistor size and keeping in pace with the CMOS developments the same trend is slowly happening in the area of MEMS in terms of rapid penetration of these devices in various domains. Silicon is the basic material in integrated circuit (IC) industry which is used for the realization of various ASICs, detectors, solar cell, radio frequency devices etc. As the MEMS processes are mostly derived from IC technology due to availability of processing infrastructure and high quality materials so silicon wafer is the natural choice in due to ease of production and integration. Silicon has a larger bandgap giving it the ability to operate at higher temperatures and ease of formation of silicon dioxide which is chemically and mechanically very stable [1].

It is most widely distributed in dusts, sands, planetoids and planets in various forms [2]. Silicon structure is classified as crystalline, polycrystalline and amorphous and mostly poly and single crystal silicon (SCS) is employed in IC realization whereas amorphous structure in which atomic position is completely random, in spite of low cost, is comparatively less efficient. Silicon wafer is either single bulk crystal or polycrystalline whereas polycrystalline wafer is expensive. Single crystal silicon is converted from high purity sand with impurity level of 1 ppb. The criteria for transistor and optoelectronic devices demands wafer to be having single crystal so as to minimize the inherent defects. The size of the silicon wafer depends on ingot and for less than 200 mm (< 8”) wafer size; one or more flat regions are ground which specifies the crystal orientation and dopant type. The ingots of silicon wafer are sliced and can be further lapped to achieve the desired thickness [3]. The typical processing steps carried out in wafer preparation are shown in Fig1.

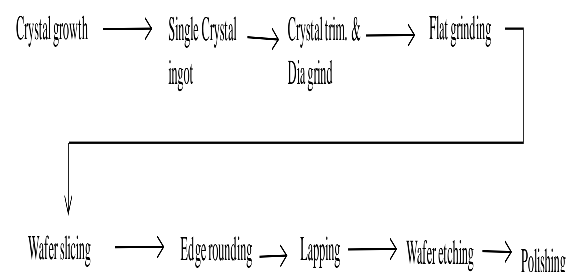

Figure1 Wafer preparation steps

Slicing determines four wafer parameters: surface orientation, thickness, total thickness variation (TTV) and bow (wafer curvature). The requirement of wafer

Cite this paper:

K.Singh, A V Nirmal, “Silicon Wafer Specifications and Its Selection Criteria”, International Journal of Advances in Computer and Electronics Engineering, Vol. 3, No. 5, pp. 9-13, May 2018.

for IC fabrication is quite different from other applications such as sensors, photovoltaic and optoelectronic devices, solar cells etc and accordingly wafer is chosen. This demand for some specific parameters to be caters for meeting the desired requirements. High-power/high-voltage devices need progressively lower resistivity silicon substrates to function efficiently and radio-frequency (RF) operating ranges, higher resistivity substrates are needed to isolate transistors and passive components. Presently most commonly employed silicon wafers are SOI, epitaxial, high resistivity (HRS) which are processed as per the requirements of specific parameters [4]. Epi and SOI wafer are created on SCS using particular technique known as Czochralski whereas high resistivity wafer uses another technique. Epitaxial wafer consists of compound semiconductor material and are mostly employed in optoelectronic and photovoltaic devices. SOI wafers apart from enhancing latch-up immunity in IC circuits are also employed in the pressure sensors fabrication to achieve precise diaphragm thickness.

This article discusses the various parameters of silicon wafers, notable difference between Epi, SOI and HRS wafer along with the potential applications. Consolidation of the various parameters and its relevance are also discussed.

2. GROWTH TECHNIQUES & GENERIC SPECIFICATIONS

Single crystal growth techniques are categorized as Czochralski (CZ) or Float zone (FZ). The preparation methodology such as growth rate, diameter, dislocation density, dopant distribution changes with the selected techniques adopted for manufacturing. Resistivity is the main difference in the high resistivity wafer. CZ and Bridgmann are mostly employed for bulk SCS whereas FZ technique having high purity is used to realize high resistivity. Mostly CZ technique is preferred due to greater control over the crystal growth process. In RF applications, high permittivity semiconductor material such as GaAs and Silicon (FZ) are employed to realize miniature microwave circuits due to ease of integration of active and passive circuits. Compared to GaAs, Si MMIC is gaining popularity as variation of dielectric constant with frequency and temperature is minimal in addition to three times higher thermal conductivity and better surface smoothness. The main parameters of the silicon wafer are the size, resistivity, smoothness, dopants apart from bow and warpage [5]. Resistivity of the wafer depends on the grain boundaries which increase with the scattering of free carriers.

RF applications require substrate having higher resistivity to minimizes the dielectric losses. Further minority carrier lifetime which governs efficiency parameters in transistors and optoelectronic devices are also dependent on the grain boundaries. Also dislocations impact in degrading the performance of the semiconductor material [6].

TABLE 1 COMPARATIVE LIST OF MATERIAL PROPERTIES

Material Property	Crystalline silicon	Poly silicon
Specific Heat(cal/g°K)	0.169	0.169
Thermal Expansion (10^{-6}/°K)	2.33	2-2.8
Mobility(cm^2/V/sec)	1500	30
Poisson ratio	0.262	0.23
Resistivity (Ω-cm)	Doping dependent	Function of grain structure

Typical parameters defining silicon wafer are:

Parameter	Unit
Type/Dopant	
▪ Resistivity	Ω cm
▪ Resistivity tolerance	
▪ Dislocations	
▪ RRV(radial resistivity)	%
▪ Oxygen	Atoms/Cm³
▪ Carbon	Atoms/Cm³
▪ Lifetime	µsec.
▪ Diameter	mm
▪ Flat, Primary	mm
▪ Flat, Secondary	mm
▪ Thickness	µm
▪ Finish	
▪ Edge rounding	
▪ TTV	µm
▪ Bow & Warp	µm

Crystals with diameters equal to or larger than 200 mm are without flats and a small groove is ground along the length of the ingot. As shown in Fig 2, 150mm wafer is having the flats for which lengths are to be defined whereas 200 mm wafer is having the notch for which notch depth and angle are to be part of the specifications.

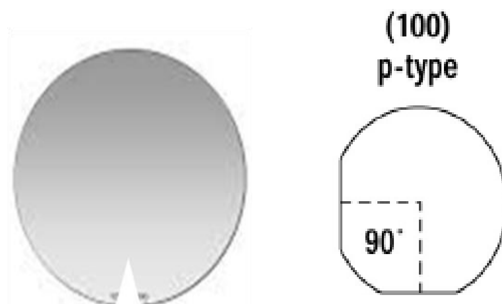

Figure 2 Typical 8" wafer (with groove) and 6" wafer (with flats)

In case of 150 mm wafer as shown in Figure 1, largest flat is called primary flat and work as a reference direction for aligning mask pattern along specific crystallographic location. Secondary flat indicates the orientation and conductivity of the wafer.

3.HIGH RESISTIVITY WAFER

The challenges for making high frequency ICs in silicon are: noise, ESD, passive component integration, modeling [7]. Low resistivity silicon used in CMOS processing is not employed in RF as parasitic electro-magnetic signal propagation through the substrate causes considerable substrate noise and cross-talk [8]. Substrate losses in silicon depends both on frequency and substrate resistivity. At low frequency, the cross talk signal from one device to another increases with frequency because of substrate coupling. Substrate resistance dominates at moderate frequencies whereas at high frequencies capacitance (permittivity) associated with silicon substrate contributes. High resistivity silicon using low doped silicon technology (Float Zone process) is also having limited isolation at multigigahertz region due to space charge region which limits the integration density due to junction isolation. But in case of lossy substrate such as CMOS grade silicon [9], the effect of dielectric and surface wave propagation are more dominant as compared to conductor losses. Various loss mechanisms encountered during signal propagation in planar lines are:

(a) Conductor losses of the metallization
(b) Substrate losses
(c) Interface losses
(d) Dielectric losses of intrinsic semiconductor
(e) Radiation losses

Effective dielectric constant depends on the frequency and substrate resistivity. The resistivity of the HR Si wafer is of the order of kohm-cm which is 100 times more compared to the standard wafer. Also the resistivity is typically defined in k ohm-cm and preferred to be higher due to reduce losses associated with the dielectric resistivity. The other parameters are same as defined for the standard wafer.

4.SOI WAFER

Silicon on insulator type of wafer is created by two processes namely silicon implanted by oxygen (SIMOX), bonded wafer and zone-melt re-crystallized (ZMR) polysilicon. It is employed for optoelectronic, RF, sensor, power and high temperature applications. In SiMOX techniques, standard silicon wafers are implanted with oxygen ions and then annealed at high temperature (1300°C). The oxide layer thickness and depth are controlled by varying the energy and dose of the implant and the annealing temperature. In fusion bonding, a layer of oxide (~1um) is grown on silicon wafer and bonded with another wafer which is annealed at ~1100°C in N_2 ambient. The mechanical grounding is carried out using polishing and CMP. Another variant i.e ZMR uses poly-silicon which is deposited on oxidized silicon wafer and re-crystallized using laser or evaporation. Other variants of the wafers are: silicon-on-glass and silicon-on-sapphire in which the traditional silicon substrate is thinned and mounted to a supporting insulating layer. Device layer and isolation layer thickness are the main parameters in the selection of the wafer apart from other generic parameters. The main parameters defined for the wafer are: doping, device layer thickness and resistivity, handle layer thickness (Fig 2).

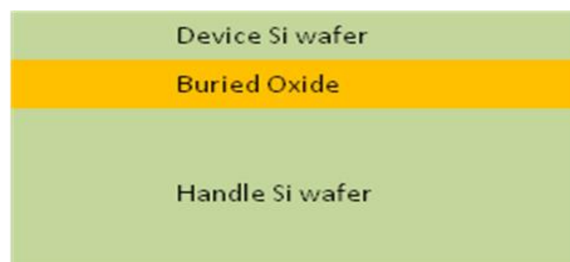

Figure 3 Cross section view of SOI wafer

The main applications of these wafers are associated with the isolation and noise reduction [10]. SOI wafers are employed in low noise phase locked loop and high isolation analog and RF switches. Other variants such as Silicon-on-quartz (SOQ) can enhance isolation at the expense of self-heating.

5.EPI WAFER

Epi wafer is classified as Homoepitaxy (same material) or Heteroepitaxy (crystallography different) using CVD or MBE process. The thickness of epi layer is dependent on temperature and time taken for thermal diffusion. The more prominent in homoepitaxy is p- on p+ as n- on n+ effects the minority carrier lifetime.

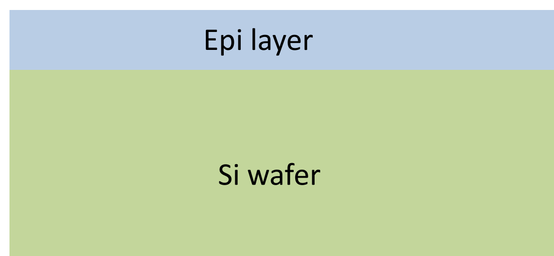

Figure 4 Cross section view of Epi wafer

Apart from generic wafer specifications the other parameters related with epi layer are: type/dopant, resistivity (Ω cm), thickness (10-20 μm). The layer

can be buried or multilayer and are grown at temperature below melting point (Fig 4). The epi layer becomes collector for transistor an element for diode or capacitor.

The main application of these wafers is to improve the latch up susceptibility of the circuit by providing shunting path for the stray current so that large current is not triggered. Apart from specific parameters, other parameters are defined as per SEMI standards. Present era is moving the wafer size from 75mm,100 mm,125mm,150mm,200mm and now 300 mm (18"/925um) which increases the weight as shown in Table-2.

TABLE 2 COMPARATIVE CHART OF WAFER SIZE VS WEIGHT

Wafer (Si) Size/Thickness	Weight (g)
4" /525µm	9.5
6"/675µm	25
8"/725µm	53.4

Also higher sized wafer is not having flats instead they are having a notch for orientation. So in MEMS structure where bulk micromachining is involved it is preferable to employ 6" wafer. Also other parameters such as OF,BMD (bulk micro defects),SFQR are defined for larger wafer size. Crystallographic originated particles are also plays an important role and depends on the crystal pulling rate which increases proportional to the pulling rate. The elimination of such particles can be carried out by annealing the wafer. All wafers undergo various processing steps which are carried out at varied temperature. Various other wafers variants such as ultrathin, refurbished are also employed as per the requirement and cost implications.

6. CONCLUSION

This article details the wafer types and parameters which are commonly employed in microelectronics processing. As the applications are varied, the approach to choose the wafer is governed by the parameters. Apart from size and thickness, the main parameter is resistivity and for radio frequency operations it plays a major role. Present trends towards smart sensors needs higher emphasis on wafer selection to achieve the desired results. Author believes that this compilation of the basic parameters will help researchers to choose the wafer according to the applications.

7. ACKNOWLEDGEMENTS

Authors gratefully acknowledge Deputy Director and Director for their support and encouragement.

REFERENCES

[1] Fisher,Seacrist & Standley," Silicon crystal growth and wafer technologies," Proceedings of IEEE, Vol 200, 2012,pp 1454-1474
[2] Prem Pal and Kazuo Sato (2017),"Silicon Wet Bulk Micromachining for MEMS," Pan Stanford Publishing
[3] C R M Grovenor (1989) ,"Microelectronic material," IOP Publishing Ltd
[4] G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat and V.K. Aatre(2011) ,"Micro and Smart Systems," Wiley India
[5] Kamaljeet Singh," Substrate Material Considerations in MEMS Processes for RF Applications," Nano & Microsystems technology, Viol 19, No7,2017,pp 428-431
[6] Ramany Revathy," X-Ray Diffaraction in Nanostructured Materials," International Journal of Advances in Computer & Electronics Engineering,Vol2,No 4,April 2017,pp 30-35
[7] Gary Breed," A comparison of RFIC Fabrication Technologies," High Frequency Electronics, March 2006, pp52
[8] R-Y Yang, C-Y Hung,Y-K Su, M-H Weng and H-W Wu," Loss characteristics of silicon substrate with different resistivities," Microwave and optical Technology Letters, Vol48, No 9, Sept 2006, pp1773-1776
[9] Kamal Benaissa,J-Y Yang,D.Crenshaw, S.Sridhar et al," RF CMOS on high resistivity substrates for system-on-chip applications," IEEE Transactions on Electronic Devices, Vol50, No3, March 2003, pp567-576
[10] J N Roy & M J Zarabi," Materials for VLSI Process,"IETE Journal of research,Vol 43,No 2&3,1997,pp 207-213

Authors Biography

Kamaljeet Singh has obtained M. Tech (Microwaves) from Delhi University in 1999 and awarded PhD in 2010. He joined ISRO Satellite center, Bangalore in 1999 where he worked in GEO-receiver. From August 2006 – Feb 2016 he was posted in Semi- Conductor Laboratory, Chandigarh and worked in the areas of RF-MEMS and sensors. He is presently working in SEG group at ISAC.

A V Nirmal obtained his B.E in Mechanical Engineering from Kerala University in 1984. He joined VSSC, Trivandrum in 1984 and has been working in ISAC since 2004. He is credited with productionzation and delivering of all sub-systems of IRS and Geosat missions. He was involved in the design and development of various mechanical systems for both Launch vehicle and satellites and establishment of test

International Journal of Advances in Computer and Electronics Engineering
Volume 3, Issue 5, May 2018, pp. 9–13

facilities. He is presently working as Group Director, Systems Engineering Group, ISRO Satellite Centre

Cite this paper:

K.Singh, A V Nirmal, "Silicon Wafer Specifications and Its Selection Criteria", International Journal of Advances in Computer and Electronics Engineering, Vol. 3, No. 5, pp. 9-13, May 2018.