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Design and Implementation of Symmetric Multilevel Inverter

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Abstract: *In this paper, an advanced configuration for a symmetric multilevel voltage source inverter is proposed. The proposed inverter is able to generate the nine levels using a lower number of circuit devices, including power semiconductor switches. Moreover, the reduced amount of on-state switches in the suggested configuration decreases voltage drops. Power losses are diminished. The given simulation results confirm the feasibility of the proposed configuration. To approve the practicability of the proposed inverter, a prototype of the proposed topology has been implemented. Finally, simulation results show that the obtained results are in good agreement. As a result, the total cost is considerably reduced, and the control scheme gets simpler.*

Keyword: *Higher efficiency; Multilevel voltage source inverter (MVSI); power losses; reduction of circuit components; symmetric inverter; voltage drop;*

1. INTRODUCTION

The main goal of Proposed Multilevel voltage source inverter (MVSI) is a practical power electronic configuration that gives higher output power quality by lowering the total harmonic distortion, also lower switching losses in order to improve efficiency [1]. In conventional symmetric multilevel inverter has ten on-state switches and ten gate driver with four dc sources. In proposed symmetric multilevel inverter has eight on-state switches and eight gate driver with same four dc sources. Hence this shows two on-state switches and its related gate driver were eliminated [2] [3]. A lower number of on-state switches result in lower power losses and voltage drops which improves efficiency [4]. The proposed symmetric multilevel inverter aims to generate the stepwise nine level output voltage waveform by synthesizing dc power supplies connected to its input terminals. Due to an increase in the number of dc source on the input side, the number of output levels increases. Multilevel inverters have found successful application in the area of high-power medium energy control and renewable energy resources. Since the introduction of multilevel inverters, different switching methods such as Pulse Width Modulation (PWM) techniques have been suggested and helps to improve the power quality of the output voltage waveform [4].

This paper suggests a new modular configuration for the symmetric MVSI. This proposed topology has been compared with conventional symmetric topologies, and the results have improves its efficiency in the way of reducing the circuit devices.. Moreover,

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the control scheme is simpler. The provided simulation results demonstrated the benefits of the introduced MVSI. To show the feasibility of the proposed multilevel inverter, the simulation studies are presented at first. This converter is simulated by MATLAB software. MATLAB software helps to found the final result of the paper in form of simulation before applying in experimental form. Finally, simulation results show that the obtained results are in good agreement.

2. CONVENTIONAL CONFIGURATION

Figure 1 shows the circuit diagram of conventional configuration. This nine level inverter has ten power semiconductor switches with four dc source [4]. The conventional configuration has power semiconductor switches such as S1, S2, S3, S4, S5, S6, S7, S8, S9 and S10 are MOSFET IRF840 with four 12V,7.5 AH battery which produce a nine level staircase output waveform. For +1 level S1, Bt1, S7, S8, S5, S4 to load were ON condition and remaining switches were at OFF condition. For +2 level S1, Bt1, S9, S10, S5, S4 to load were ON condition and remaining switches were at OFF condition. For +3 level S1, Bt1, Bt2, S9, Bt3, S8, S5, S4 to load were ON condition and remaining switches were at OFF condition. For +4 level S1, Bt1, Bt2, S9, Bt3, S8, S5, Bt4, S3, S4 to load were ON condition and remaining switches were at OFF condition. For zero level all dc sources were at OFF condition. For -1, -2, -3, and -4 level same switches were at ON and OFF conditions but the battery terminals were opposite side. Hence nine level staircase output waveform be attained.

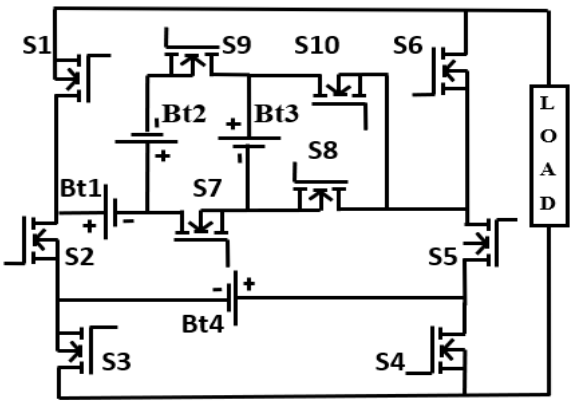

Figure 1 Circuit diagram of conventional configuration

3. PROPOSED CONFIGURATION

Figure 2 shows the circuit diagram of proposed configuration. This nine level inverter has eight power semiconductor switches with four dc source. The conventional configuration has power semiconductor switches such as S1, S2, S3, S4, S5, S6, S7 and S8 are MOSFET IRF840 with four 12V, 7.5AH battery which produce a nine level staircase output waveform. From the comparision between conventional and proposed configuration, two power semiconductor switches were reduced. The reducing amount of power semiconductor switches improves efficiency by reducing switching losses. For +1 level S1, Bt1, S5, S6, S2 to load were ON condition and remaining switches were at OFF condition. For +2 level S1, Bt1, S5, Bt4, S8, S2 to load were ON condition and remaining switches were at OFF condition. For +3 level S1, Bt1, Bt2, S7, Bt3, S6, S2 to load were ON condition and remaining switches were at OFF condition. For +4 level S1, Bt1, Bt2, S7, Bt3, Bt4, S8, S2 to load were ON condition and remaining switches were at OFF condition. For zero level all dc sources were at OFF condition. For -1, -2, -3, and -4 level same switches were at ON and OFF conditions but the battery terminals were opposite side. Hence nine level staircase output waveform be attained.

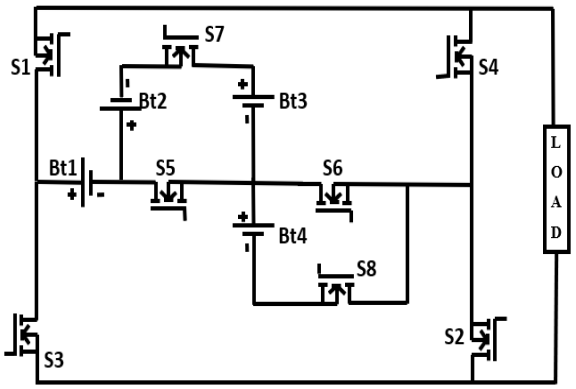

Figure 2 Circuit diagram of proposed configuration

4. SOFTWARE DESCRIPTION

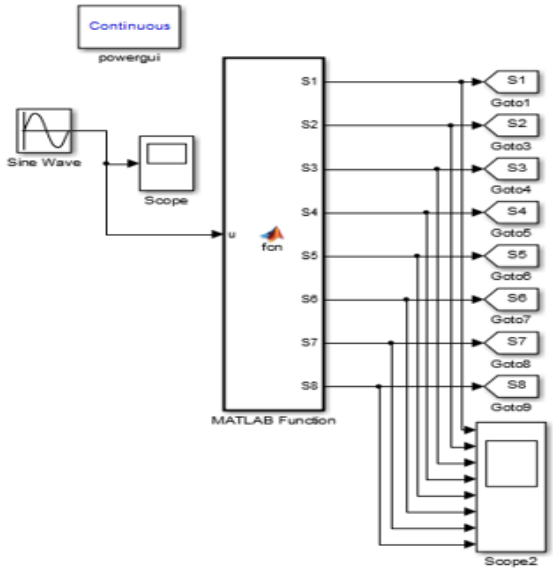

Figure 3 Circuit to generate pulse from MATLAB function

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The software used in this paper was MATLAB. With the help of MATLAB software we simulate the circuit and obtained output waveforms before applying experimental form. The simulation circuit to generate pulse from MATLAB function as shown in Figure 3. Powergui is a power supply for whole circuit where sine wave gives 50Hz ac supply. Scope is the parameter that helps to show the output waveform. MATLAB function contains coding that helps to generate on-off pulse to go to switches. These go to switches transmits the ON-OFF condition to the from to switches in Figure 4. These switches were ON condition in some cases and OFF condition in some cases where based on coding in MATLAB function. This circuit has R-L load where 20ohm and 18H. The output voltage waveform and output current waveform as shown with the help of scope parameter.

The simulation circuit to link the generated pulse to switches as shown in Figure 4. The generated on-off gate pulse links from goto switches to fromto switches. Voltage measurement parameter and current measurement parameter were connected to the circuit in order to found the voltage and current in the circuit. DC1, DC2, DC3 and DC4 are the dc battery sources having each of 12V,7.5AH.

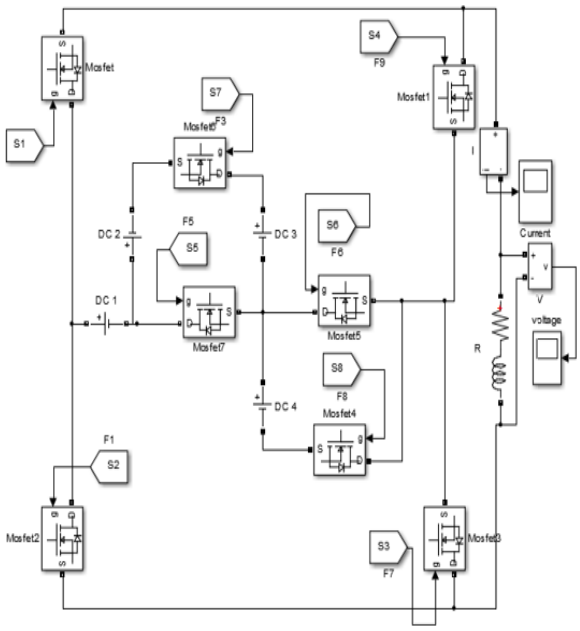

Figure 4 Circuit to link generated pulse to switches

5. SWITCHING STATES

Switching states is the digital electronics study of properties of switches, in which their output state is only a function of present state. Switches are considered as having only two exclusive states, open or closed. It is necessary to account both open and closed switch at a time period. The switch case action subsystem is a block preconfigured as a starting point for creating subsystem whose execution is triggered by a switch case block. Table 1 switching states gives the required nine level output waveform, for +1Vdc S1, S3, S5, S6 are ON condition and remaining switches were at OFF conditions. for +2Vdc S1, S3, S5, S8 are ON condition and remaining switches were at OFF conditions. for +3Vdc S1, S3, S6, S7 are ON condition and remaining switches were at OFF conditions. for +4Vdc S1, S3, S7, S8 are ON condition and remaining switches were at OFF conditions. for 0Vdc S3, S4 are ON condition and remaining switches were at OFF conditions. for -1Vdc S2, S4, S5, S6 are ON condition and remaining switches were at OFF conditions. for -2Vdc S5, S8 are ON condition and remaining switches were at OFF conditions. for -3Vdc S1, S3, S5, S6 are ON condition and remaining switches were at OFF conditions. for -4Vdc S6, S7 are ON condition and remaining switches were at OFF conditions. Its simulation output were shown on the upcoming pages.

TABLE I SWITCHING STATES OF PROPOSED SYMMETRIC NINE LEVEL INVERTER

Voltage Levels	**Switches**							
Vdc	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**
+1Vdc	1	0	1	0	1	1	0	0
+2Vdc	1	0	1	0	1	0	0	1
+3Vdc	1	0	1	0	0	1	1	0
+4Vdc	1	0	1	0	0	0	1	1
0Vdc	0	0	1	1	0	0	0	0
-1Vdc	0	1	0	1	1	1	0	0
-2Vdc	0	0	0	0	1	0	0	1
-3Vdc	0	0	0	0	0	1	1	0
-4Vdc	0	0	0	0	0	0	1	1

6. SIMULATION RESULTS

Simulation results shows the output pulse waveforms at different levels also shows output voltage waveform of nine level inverter and output current waveform of nine level inverter. Figure 5 shows the output pulse waveform at different levels. The pulse of S1, S2, S3, S4, S5, S6, S7 and S8 were different because of coding the program in MATLAB function for attaining multilevel output waveform. Figure 6 shows the output voltage waveform of nine level inverter. This shows the nine level staircase output waveform. Figure 7 shows the output current waveform of nine level inverter.

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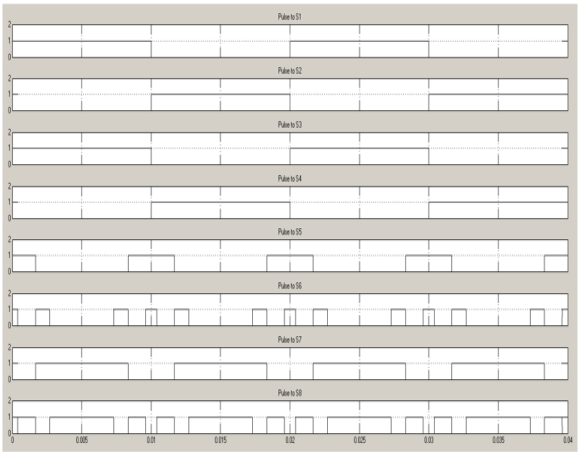

Figure 5 Output pulse waveform at different levels

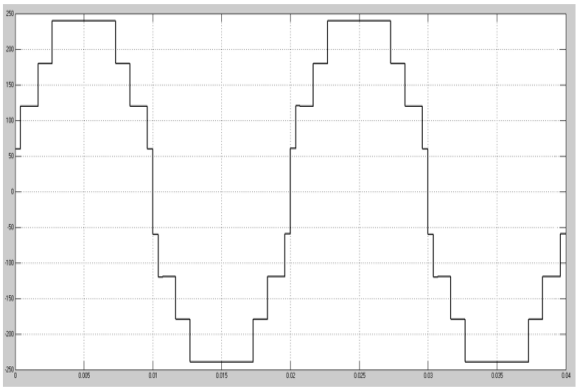

Figure 6 Output voltage waveform of nine level inverter

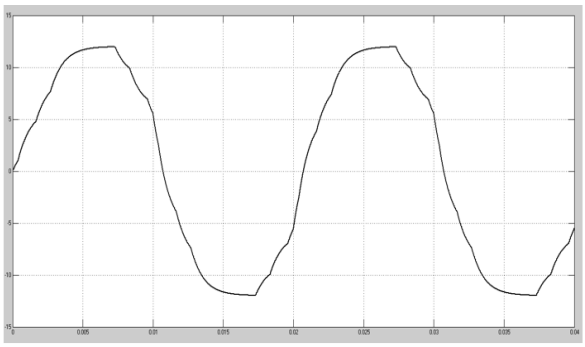

Figure 7 Output current waveform of nine level inverter

8. CONCLUSION

The contribution of this paper has been to propose an advanced configuration for symmetric inverter. This paper uses a reduced number of devices, including its power semiconductor switches. The suggested multilevel inverter has lowest amount of power losses when compared to conventional topology [4]. The lower number of devices results in substantial reduction in total costs and a simpler control scheme. Finally simulation results were obtained successfully.

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