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Design of Low Power ALU Architecture based on SRGDI Primitives

Sabapathy Arumugam Sivakumar
Assistant Professor, Department of ECE, Info Institute of Engineering, Coimbatore, India
Email: siva3cool@gmail.com

Muruganatham Haritha
UG Scholar, Department of ECE, Info Institute of Engineering, Coimbatore, India
Email: harithamuruganatham@gmail.com

Ramachandiran Gowthamkrishna
UG Scholar, Department of ECE, Info Institute of Engineering, Coimbatore, India
Email: gowthamkrishnahar@gmail.com

Karthega Arul
UG Scholar, Department of ECE, Info Institute of Engineering, Coimbatore, India
Email: karthegachetty6288@gmail.com

Abstract: *Improvement in GDI (Gate Diffusion Input) techniques have achieved major milestones such as reduction in power, reduced area and reduction in switching activities. SRGDI (Self-Resetting GDI logic) is the advanced technique used by VLSI researchers in sequential circuits. So the purpose of this paper is to design 8-bit ALU using SRLGDI technique. This ALU contains full adder, half adder, 4X4 multiplier, comparator, AND, NAND, OR and NOR gates. Comparative analysis is to be performed with other existing CMOS techniques. The earlier and the proposed SRLGDI based ALU will be simulated using Tanner EDA with IBM 130nm CMOS technology*.

Keyword: *ALU, CMOS, GDI, SRLGDI, and Switching activity.*

1. INTRODUCTION

The recent VLSI technology reduces the power consumption, delay, number of transistors by implementing low power techniques this paper goes through a study on the Self Resetting Gate Diffusion Input (SRGDI) logic for the power reduction and delay in VLSI circuits solving several problems in dynamic CMOS circuits. Sometimes due to high operating frequency the power dissipation increases. To overcome this drawback there comes a Pass Transistor Logic (PTL). This PTL logic is said to be a dynamic CMOS logic and it is used for high speed applications due to its better performance. However, this PTL logic has some drawbacks like noise immunity and large propagation delay this can be resolved by SRGDI techniques. Self-resetting GDI circuit automatically reset themselves after a period of delay [1-2]. SRGDI is a asynchronous dynamic circuit

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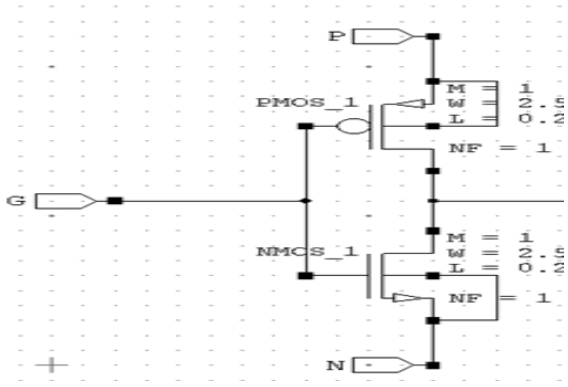

Figure 1 Structure of basic GDI cell

In this logic, it automatically resets the input with an given interval of clock pluses. SRL represents signals as short-duration pulses rather than as voltage levels. Our proposed idea is to design SRGDI primitives, adders, multiplier and comparator and implement them in 8-bit ALU.An ALU is a fundamental building block of many circuits like central processing unit, graphics processing unit, etc. An ALU has some

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processor which divides into two units such as arithmetic unit and logic unit. In general, ALU includes the storage places for input operands, accumulator and shifted results.

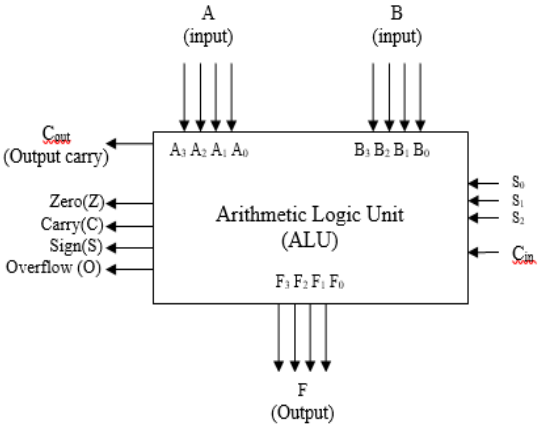

Figure 2 Structure of basic ALU

2. PROPOSED SRGDI PRIMITIVES FOR SRGDI ALU

2.1 AND GATE

AND Gate is a logical gate and it is a combination of two signals. This gate works or operates on logical multiplication rules. The AND gate is a basic digital logic gate that implements logical conjunction it behaves according to the truth table. The function can be extended to any number of inputs. In this gate if the inputs is 0, then the output is also 0, but if all the inputs are 1 the output will also be 1. AND gate performs multiplication operation of binary digits [2]. We also know there are two binary digits 1 and 0. In multiplying 0 with 0 we will get 0, 1 with 0 or 0 with 1 we will get 0. Only we get 1 when 1 is multiplied by 1.The primitive cell diagram of SRGDI AND gate is shown in Figure 3 respectively.

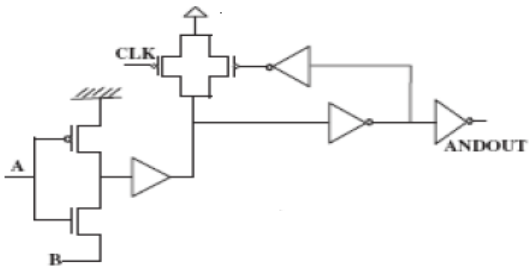

Figure 3 Primitive cell of SRGDI AND gate

2.2 NAND GATE

The NAND gate are said to be one of the universal gate in Boolean algebra and it also act as an inverter of an AND gate. The non-inverting gates do not have any versatility .A NAND Gate is a gate which is of opposite of an AND logic gate. It is a combination of AND and NOT gates and is a commonly used logic gate . Its output is complement to that of the AND gate. When 0 output results only if both the inputs to the gate are 1, if one or both inputs are 0 output results as 1[5]. The primitive cell diagram of SRGDI NAND gate is shown in Figure 4 respectively.

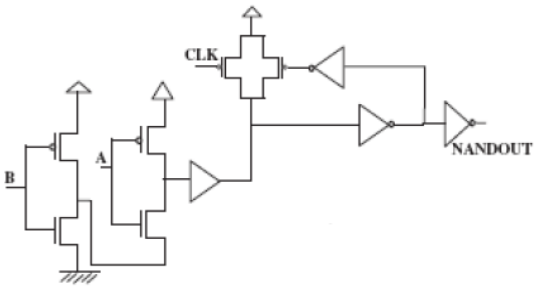

Figure 4 Primitive cell of SRGDI NAND gate

2.3 OR GATE

OR gate produces 0 output only when both the inputs are 0, in all other conditions, the output of OR gate will be 1.An OR gate is an complement of NOR gate. An OR gate performs like two switches in parallel , so that when either of the switches is closed. the light is on. An OR gate is a electrical circuit and it implements logical disjunction and also it behaves according to the truth table. The primitive cell diagram of SRGDI OR gate is shown in Figure 5 respectively [3-4].

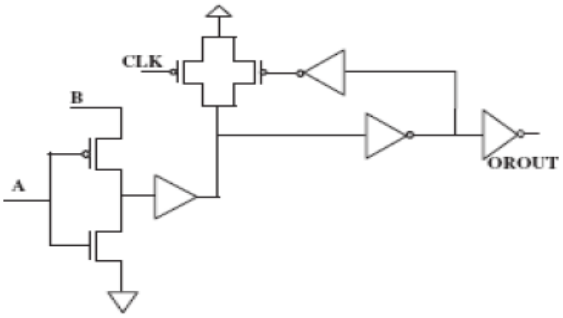

Figure 5 Primitive cell of SRGDI OR gate

2.4 NOR GATE

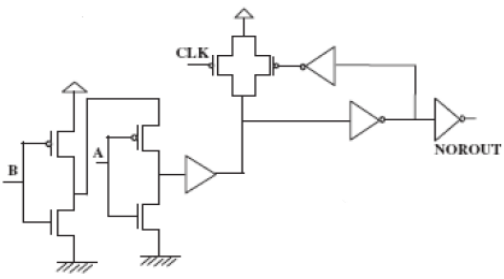

Figure 6 Primitive cell of SRGDI NOR gate

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The NOR gate is said to be the complement of OR operator. It only returns a low or high value in the absence of both input operators. The NOR logic gates are defined as the "primary" logic gates because they can produce the results of the other gates such as OR and XOR. A NOR gate works on the principle of neither this nor that. The NOR gate is a digital Logic gate and it behaves according to the truth table. The primitive cell does not diagram of SRGDI NOR is gate shown in Figure 6 respectively.

2.5 HALF ADDER

Half adder is a combinational circuit that has two inputs and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum is the (S) bit and carry is the (C) bit. A half adder circuit can be easily constructed using one X-OR gate and one AND gate. Half adder is the simplest of all adder circuit, since it has an major advantage. A half adder is an electronic circuit that performs the addition of numbers [6-7]. The half adder is able to add two single binary digits and provide the output as sum plus a carry value. The primitive cell diagram of SRGDI Half Adder is shown in Figure 7 respectively.

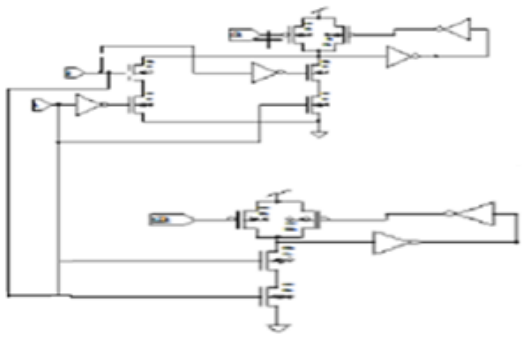

Figure 7 Primitive cell of SRGDI Half adder

2.6 FULL ADDER

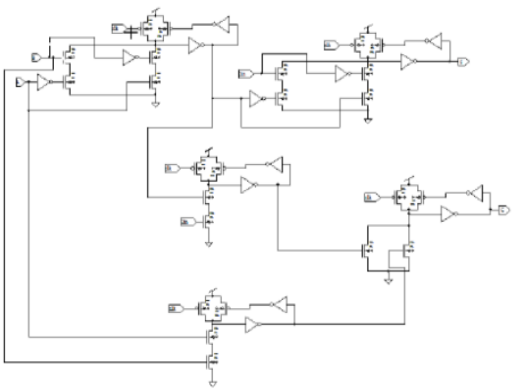

Figure 8 Primitive cell of SRGDI Full adder

Full adder which is used to add three bits and obtain a SUM and a CARRY outputs. It mainly needed to add large number of bits. The sum under of the LSB is recorded and the carry is forwarded to the next bits. Same things happen to other bits until the MSB is reached. It is a digital circuit which performs addition. Full adders are implemented with logic gates in hardware. A full adder adds three 1-bit binary numbers, two operands and a carry bit. The outputs have a sum and a carry bit. The full adder is a component in a cascade of adders, which add the binary numbers of 8, 16, etc. The primitive cell diagram of SRGDI Full Adder is shown in Figure 8 respectively.

2.7 MULTIPLIER

A multiplier is an electronic circuit used in digital electronics, to multiply binary numbers. It is built using binary adders. Various arithmetic functions can be used to implement a digital multiplier. The basic block of the multiplier is the full adder cell, thus it has an effect on the overall performance and speed of the multiplier. The primitive cell diagram of SRGDI multiplier is shown in Figure 9 respectively.

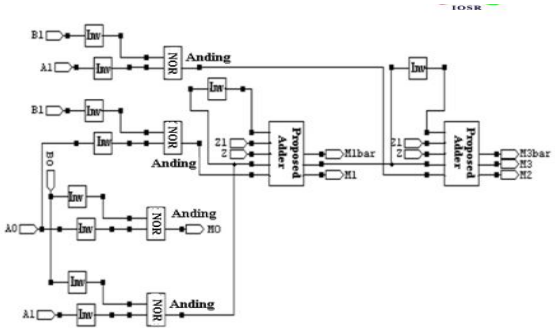

Figure 9 Primitive cell of SRGDI Multiplier

2.8 COMPARATOR

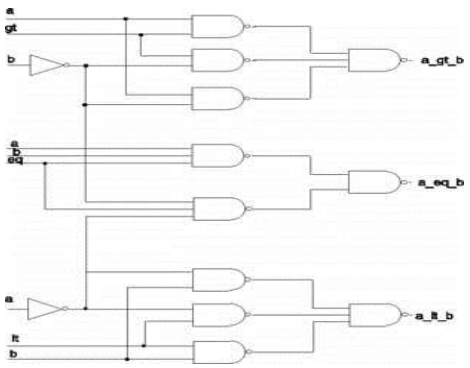

Figure 10 Primitive cell of SRGDI comparator

A comparator is used to compare a measurable quantity with a two voltages or currents. Ana log De-

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vices produces an extensive portfolio of high speed and low power comparators and this allows us to provide with more complete signal chain solutions. Comparator offers arrange from the fastest Si-based comparator to very low power CMOS comparators that consume only microamperes of power. The primitive cell diagram of SRGDI comparator is shown in Figure 10 respectively.

3. PROPOSED SRGDI ALU ARCHITECTURE

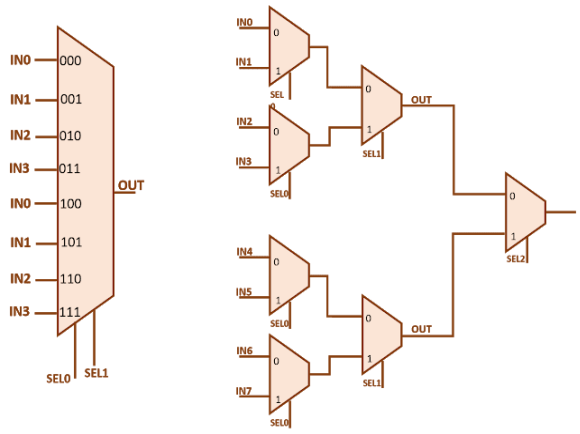

Figure 11 Primitive cell of MUX

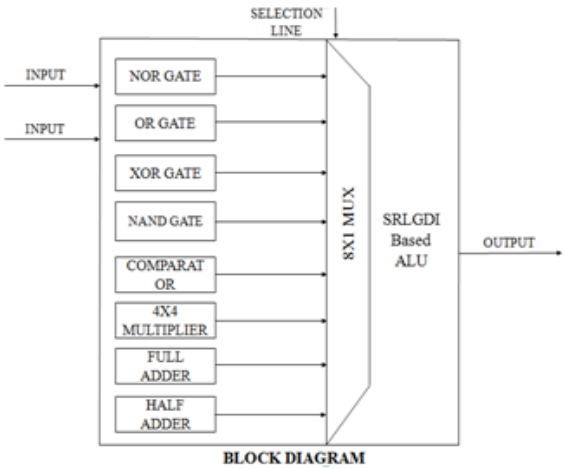

Figure 12 Bock diagram of SRGDI ALU

A multiplexer is a combinational circuit that selects one out of multiple input signals depending upon the state of select line. A 2^N:1 multiplexer with 'N' select lines can select 1 out of 2^N inputs. In other words, the multiplexer connects the output to one of its inputs based upon the value held at the select lines. A multiplexer (or commonly called as MUX) is also termed as data selector. Common functions of a multiplexer include concentrating the primitive cell diagram of MUX and block diagram of ALU is shown in Figure 11 and Figure 12 respectively.

3.1 NOR GATE

The simulation of SRGDI NOR primitive is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI NOR primitive cell is shown in Figure 13 and Figure 14 respectively.

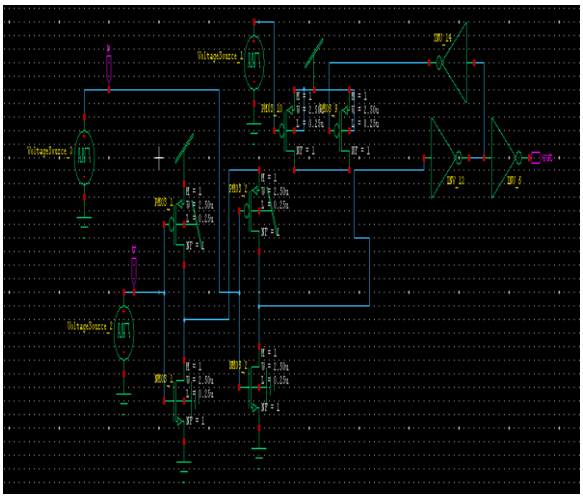

Figure 13 S-edit schematic cell of SRGDI NOR gate

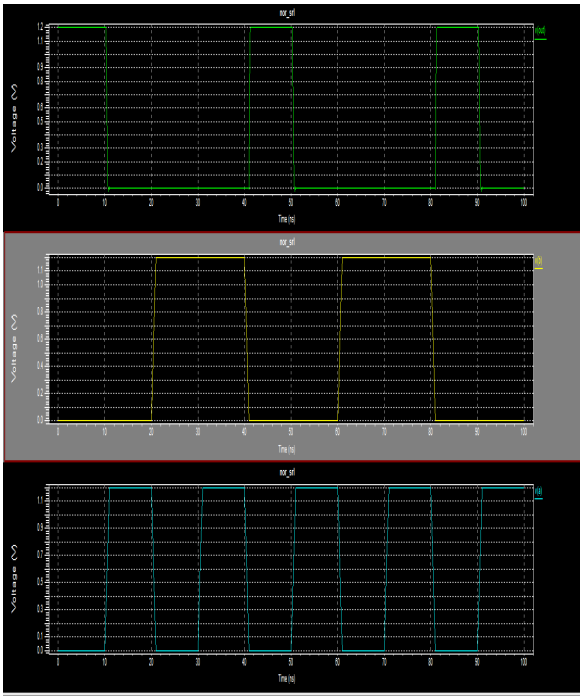

Figure 14 W-edit output waveform of SRGDI NOR gate

3.2 OR GATE

The simulation of SRGDI OR primitive is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI OR primitive cell is shown in Figure 15 and Figure 16 respectively.

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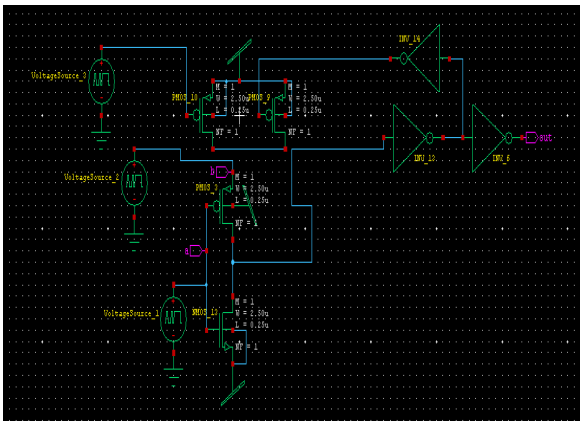

Figure 15 S-edit schematic cell of SRGDI OR gate

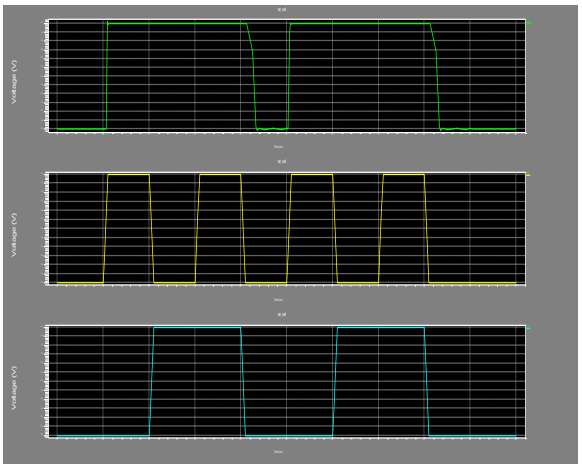

Figure 16 W-edit output waveform of SRGDI OR gate

3.3 AND GATE

The simulation of SRGDI AND primitive is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI AND primitive cell is shown in Figure 17 and Figure 18 respectively.

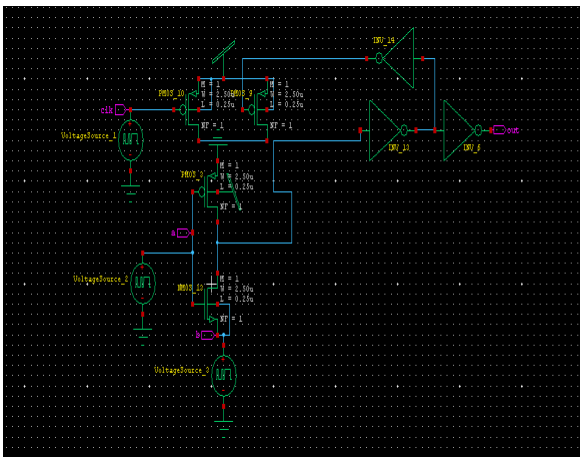

Figure 17 S- edit schematic cell of SRGDI AND gate

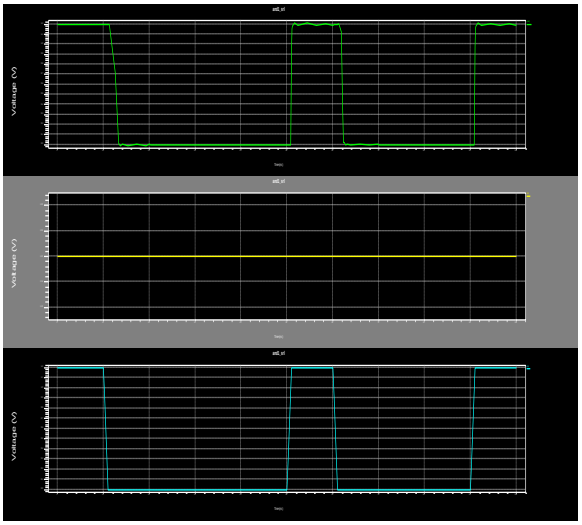

Fig.18 W-edit output waveform of SRGDI AND gate

3.4 NAND GATE

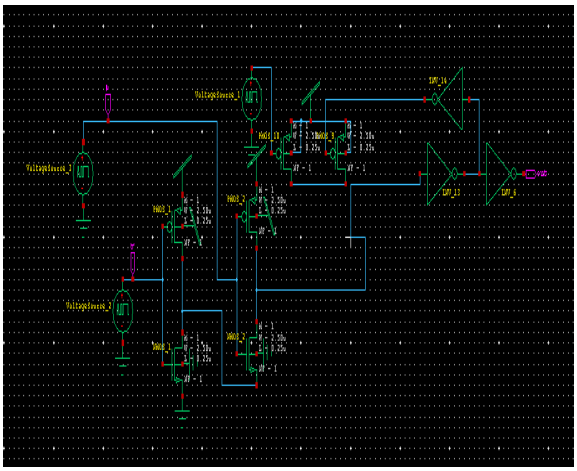

Figure 19 S-edit schematic cell of SRGDI NAND gate

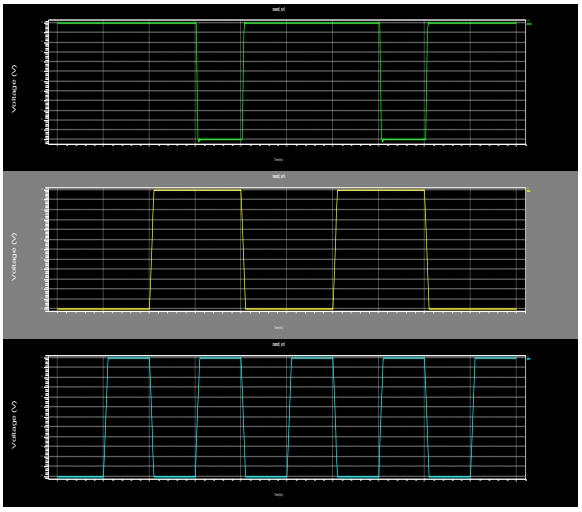

Figure 20 W-edit output waveform of SRGDI NAND gate

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The simulation of SRGDI NAND primitive is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI NAND primitive cell is shown in Figure 19 and Figure 20 respectively.

3.5 HALF ADDER

The simulation of SRGDI Half Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI Half Adder cell is shown in Figure 21 and Figure 22 respectively.

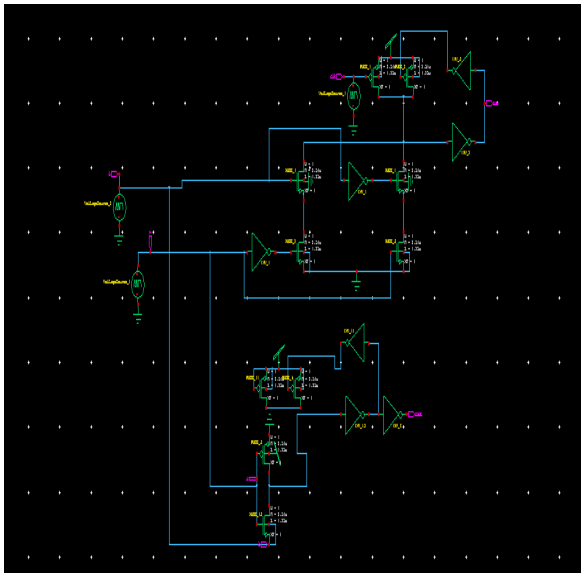

Figure 21 S-edit schematic cell of SRGDI Half Adder

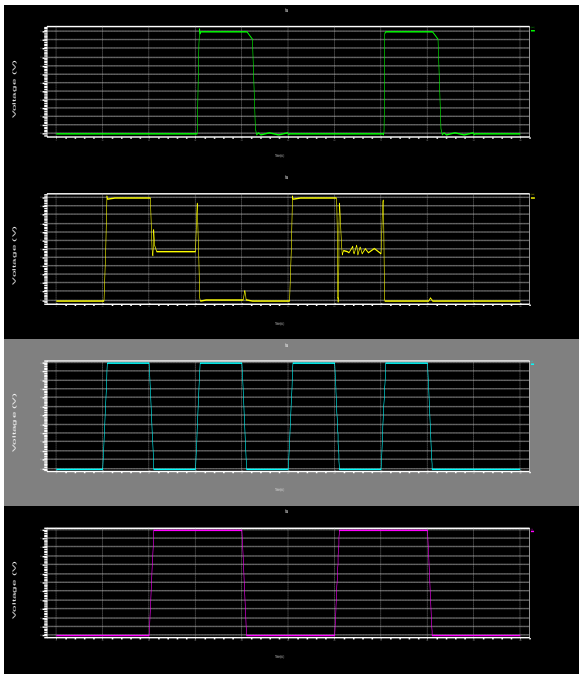

Figure 22 W-edit output waveform of SRGDI Half Adder

3.6 FULL ADDER

The simulation of SRGDI Full Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI Full Adder cell is shown in Figure 23 and Figure 24 respectively.

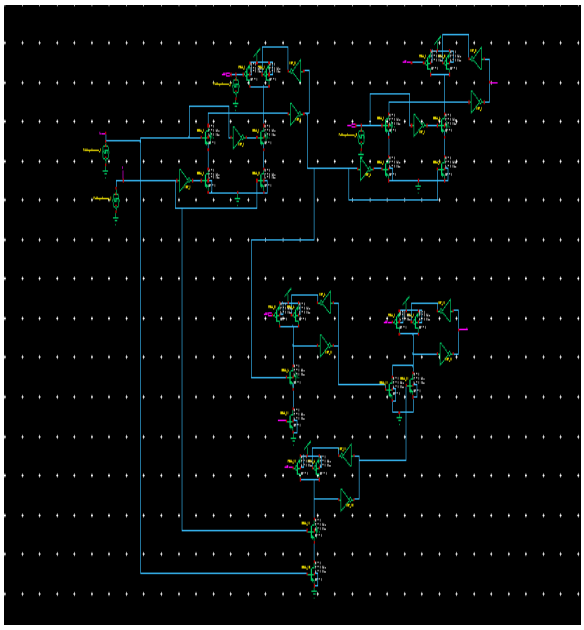

Figure 23 S-edit schematic cell of SRGDI Full Adder

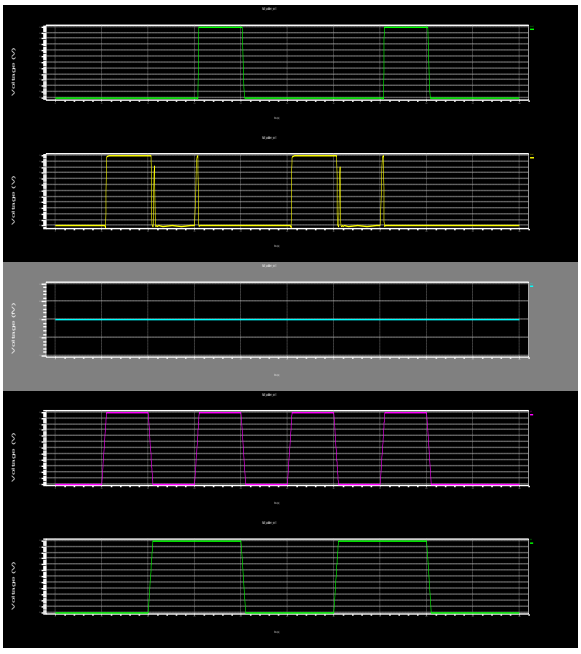

Figure 24 W-edit output waveform of SRGDI Full adder

3.7 MULTIPLIER

The simulation of SRGDI Multiplier is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output

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waveform of SRGDI Multiplier cell is shown in Figure 25 and Figure 26 respectively.

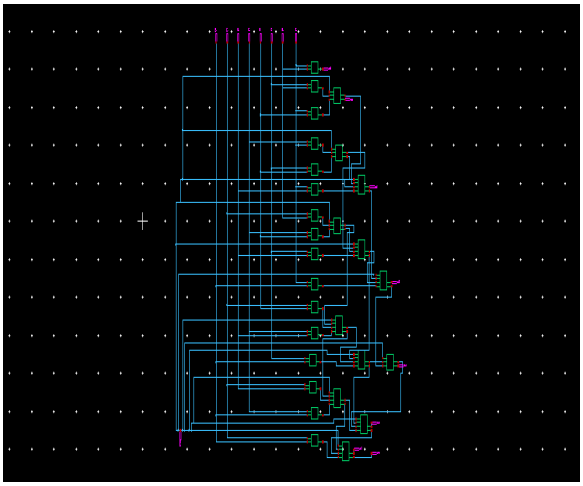

Figure 25 S-edit schematic cell of SRGDI Multiplier

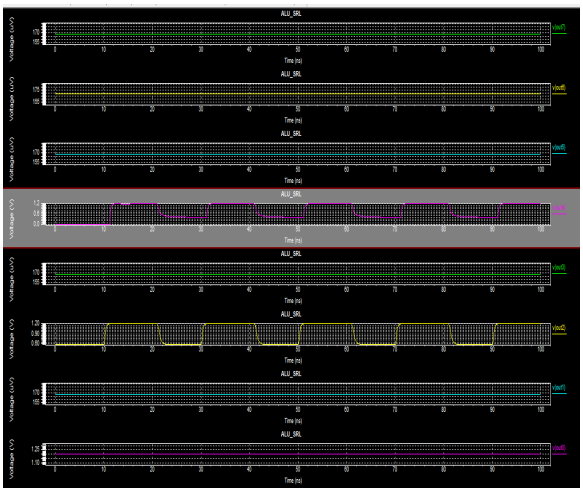

Figure 26 W-edit output waveform of SRGDI Multiplier

3.8 COMPARATOR

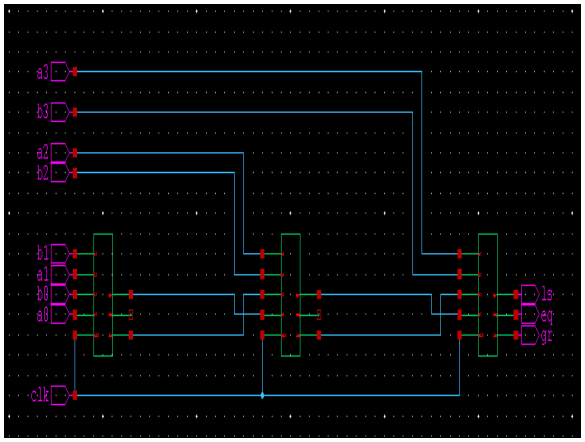

Figure 27 S-edit schematic cell of SRGDI Comparator

The simulation of SRGDI Comparator is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of SRGDI Comparator cell is shown in Figure 27 and Figure 28 respectively.

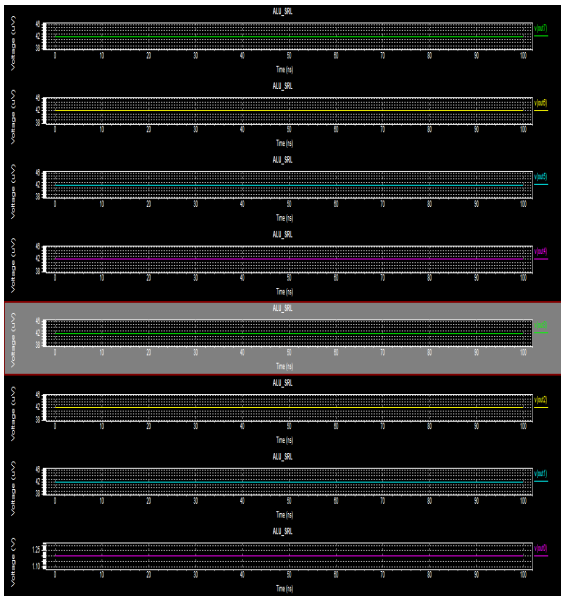

Figure 28 W- edit output waveform of SRGDI Comparator

3.9 ALU

The simulation of SRGDI ALU is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W- edit output of SRGDI ALU is shown in Figure 29 and Figure 30 respectively.

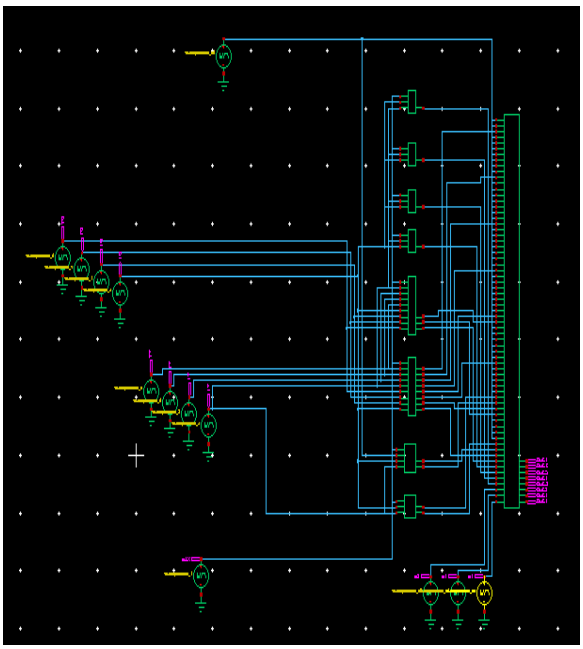

Figure 29 S-edit schematic cell of SRGDI ALU

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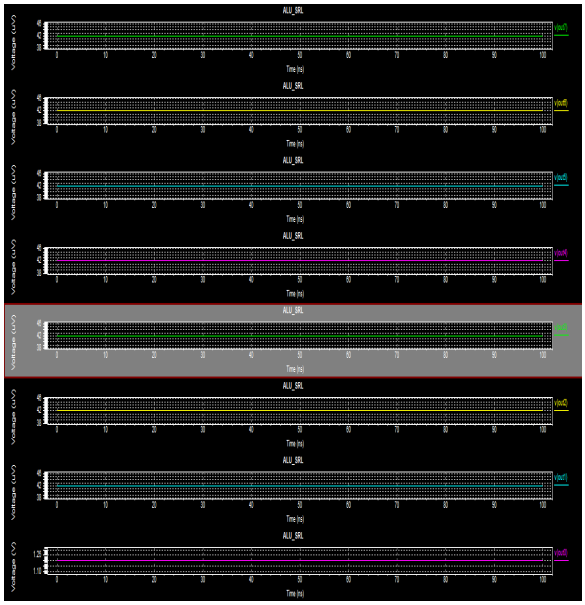

Figure 30 W- edit output waveform of SRGDI ALU

4. COMPARISON AND RESULTS

Simulations are performed using Tanner EDA using 130nm technology nodes. The analysis shows reduced power, delay and PDP for proposed SRGDI logic compared to GDI, MGDI and FSGDI approaches. The simulation results are tabulated in Table I.

TABLE I SIMULATION RESULT SHOWING PROPOSED ALU PARAMETERS

Parameters	Power (µW)	Delay (µs)	PDP (pJ)
NOR	3.153	0.26	0.819
OR	3.154	0.26	0.820
XOR	3.155	0.26	0.820
NAND	3.156	0.26	0.820
COMPARATOR	3.157	0.26	0.821
MULTIPLIER	3.158	0.26	0.821
FULL ADDER	3.159	0.26	0.821
HALF ADDER	3.160	0.26	0.822
Proposed ALU	19.86	1.24	24.62

From the above table it is clear that the proposed SRGDI ALU design shows considerable improvements in power and delay.

5. CONCLUSION

A new technique based on GDI SRL was proposed with advantage of low power consumption to existing technique. The proposed design can be used in low power logic circuits due to its low power, low device count. The proposed SRLGDI ALU logic performs better than different logic and its existing counterparts. While comparing the other techniques like adiabatic logic represents average power of 4.93, our proposed method SRLGDI represents low power of 4.60 as a whole. On the whole about 45% of power and 39% of PDP have been achieved using this proposed SRLGDI logic when compared with the existing logics.

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Authors Biography

Sivakumar Sabapathy Arumugam has a B.E., degree in ECE and M.E., degree in VLSI Design and working as Assistant Professor at Info Institute of Engineering Coimbatore, India. He is pursuing his Research in Anna University- Chennai. His areas of interests are VLSI design and embedded systems.

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Gowthamkrishna Ramachandiran is pursuing B.E., degree in ECE at Info Institute of Engineering Coimbatore- India. His areas of interests are VLSI design and embedded systems.

Haritha Muruganatham is pursuing B.E., degree in ECE at Info Institute of Engineering Coimbatore-India. Her areas of interests are VLSI design and embedded systems.

Karthega Arul is pursuing B.E., degree in ECE at Info Institute of Engineering Coimbatore-India. Her areas of interests are VLSI design and embedded systems

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