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Mathematical Model of Energy Consumption of A Hierarchical Shared Bus Interconnection Communication Network of an On-Chip Multiprocessor

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Abstract: *Energy consumption is one of the performance issues in multiprocessor design. Apart from being critical for power critical systems, it determines the amount of heat dissipates by the system. That is, as the energy consumption rate reduces heat dissipation reduces. Many research efforts had gone into the different design schemes for reducing multiprocessors' energy consumption. However, it has been observed that there is a distinct relationship between energy consumed and the interconnection network engaged by the multiprocessors. In this paper, an energy consumption model was developed for a bus based interconnection network multiprocessor. The model established a linear relationship between bit energy of multiprocessor shared bus interconnection network and length of the bus covered during the bus cycle. This was used to obtain the maximum energy and bit energy consumed by the multiprocessor. The obtained bit energy (Pwbit) was compared with the bit energy of other interconnection networks in order to determine and evaluate the interconnection network which consumes least energy during bits transition. The bit energy obtained (2.45x10-21 J) for the hierarchical shared bus interconnection network was much lower than the results reported for Crossbar (2.2 x 10-13 J), Banyan 2x2 (1.1 x 10-12 J), Batcher 2x2 (1.2 x 10-12 J), Banyan 4x4 (1.4 x 10-14 J), Banyan 16x16 (1.5 x 10-14 J) and Banyan 32x32 (2.2 x 10-14 J) interconnection networks. This indicates that the use of hierarchical shared bus interconnection network in the multiprocessor reduces its energy consumption.*

Keyword: *Energy consumption; multiprocessor; interconnection network (IN); shared bus*

1. INTRODUCTION

The modern multiprocessor systems design shows a clear trend toward integration of multiple processors. Presently embedded applications are migrating from single processor systems to multiprocessor systems which have higher processing power. This development is due to the performance demanded by some of these applications which could only be met by the use of multiprocessors. Multiprocessor systems contain complex communication interconnection, such as hierarchical buses, crossbar, and banyan interconnection networks which contribute to energy consumption and performance of the system [1][2]. Apart from this, multiprocessor architectures have some other features which make them different from uniprocessor architectures. These include processing patterns, processor-memory-hierarchy, scheduling and load balancing technique. The trend of development in some of these features is accelerating faster due to increase in the computational power demanded by embedded applications [3]. One of the highly improving features of multiprocessor architecture is the Interconnection Network (IN). There are various types of INs engaged by multiprocessors' designers. Some are considered for their application specificity while some for their simplicity.

Interconnection network wire materials could be polysilicon, aluminum, copper or diffusion materials

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(n+/p+). There are different factors which militate against the functionality of wire. These factors are called wire parasites. These parasites are capacitive, resistive and inductive parasitic effects of wire. It should be noted that these parasitic effects affect circuit performance by contributing to energy dissipation and power distribution, introducing extra noise sources which affect circuit reliability and increasing the signal propagation delay. Any of the wire parasites can be used to model energy consumption of the IN. However, for multiprocessor interconnection, it is ideal to model the interconnect wire using the parasitic capacitance and neglect the inductive parasitic effect of the wire due to the fact that capacitance parasitic effect is more dominant in bus interconnection than inductive parasitic effect [4]. The parasitic capacitance effects on a unit bus length can be modeled as a capacitor to the ground. The fact that significant energy is consumed on the multiprocessor network, therefore having a pre-knowledge of the energy consumption of some of the existing interconnections would in no small means aid efficient multiprocessor design.

The remaining part of this paper is arranged as follows: section 2 contains reviews of some related works on modeling of multiprocessor interconnection networks. The mathematical model for the hierarchical bus interconnection network was presented and evaluated using different data sizes and bus lengths in section 3. Section 4 is the conclusion and recommendation.

2. RELATED WORKS

Recently, the focus has been on the reduction of the processors' power consumption rate. It has been discovered that 80-85% percentage of power consumed by multiprocessor is on the multiprocessor's interconnection network during bus cycle [4][5]. This implies that an efficient IN in terms of power consumption rate will produce multiprocessor with low power consumption rate [5]. Therefore, in order to determine and choose a low power consumption rate IN for multiprocessors, researchers have developed different power models to characterize the power profile of the interconnection networks [6].

In [7], different tightness of unidirectional graphs were modeled to determine the best tightness and some invariants of graph useful in the analysis of multiprocessor interconnection networks. The results showed that the number of connected graphs with bounded tightness is finite. In [7] a generic traffic model for on-chip interconnection networks was proposed. This traffic model is based on three empirically derived statistical characteristics using temporal and spatial distributions. With captured parameters, the model generated accurate traffic patterns recursively to show similar statistical characteristics of the observed on-chip networks. The model, which was defined by capturing statistics, can be used to reproduce any kind of on-chip interconnection traffic patterns.

Authors in [8] proposed an alternative interconnection network which is based on the Tapered Fat Tree (TFT) topology. The latency and power efficiency were evaluated. It was observed that, the benchmarks that exhibited large amounts of off-chip traffic completed a workload up to 33.6% faster on the TFT than the same workload on the mesh. Apart from this, the results showed that TFT topology has a better energy efficiency in all cases. At the cost of extra design complexity, the results suggest that the TFT topology offers better latency, throughput, and energy-efficiency overall than the mesh for memory-intensive applications running on manycore processors [8].

Apart from energy consumption model, a traffic model to characterize an application-specific network is necessary. In [9] a generic traffic model for on-chip interconnection networks was proposed. With captured parameters, the proposed model could generate accurate traffic patterns recursively to show similar statistical characteristics of the observed on-chip networks. Another important design issue of synthesizing the most power efficient Network on Chip (NoC) interconnect for CMPs was highlighted in [10]. In their synthesis approach, an accurate delay and power models for the network components (switches and links) that are obtained from layouts of the components using industry standard tools was employed. The synthesis approach utilizes the floorplan knowledge of the NoC to detect timing violations on the NoC links early in the design cycle. This led to a faster design cycle and quicker design convergence across the high-level synthesis approach and the physical implementation of the design. The design flow predictability of the proposed approach was done by performing a layout of the NoC synthesized for a 25-core CMP [10]. In [11], the use of history based dynamic voltage scaling (DVS) for links was presented. In DVS the frequency and voltage of links are dynamically adjusted to minimize power consumption. A history-based DVS policy judiciously adjusts link frequencies and voltages based on past utilization. According to the results of the experimentation the approach realized up to 6.3X power savings (4.6X on average).

3. MODELING POWER CONSUMPTION OF SHARED BUS INTERCONNECTION NETWORK

Power consumption in the multiprocessor system network comes from internal node switches, interconnected wires, and the internal buffers [12]. In this section the power consumption model of a hierarchical shared bus interconnection network used in the multiprocessor shown in Figure 1, was modelled. The multiprocessor employs a shared bus topology with no switch because not more than one processing ele-

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ments in a cluster transmit at a time, therefore, no contention and collision. The processing element(s) receives partially executed data from adjacent processing element during macro pipeline execution through inter and intra memory communication schemes. The major source of power consumption during data transition is through interconnected wires. This is modelled as wire bit energy (P_{wbit}); this is the energy or power consumed when a bit is transmitted from one point to another through a wire. β is the activity factor which is the rate of bit change in traffic. This is represented as the rate at which the capacitor in the model is charging and discharging. The maximum bit energy is consumed when bit(s) is transferred through maximum bus or wire length [12][13].

From Figure 1, the maximum wire length that could be spawned during communication occurs when there is intercommunication between the first cluster and the last cluster, which spans through $2*W_{intra\ AMBA\ bus} + W_{inter\ AMBA\ bus} + 2*W_{bridge} + 2*W_{shared\ memory\ bus}$. If the multiprocessor communication bus is modelled as a capacitor, then the equivalent maximum wire that can be spanned is either AF or GH, as shown in Figures 2 and 3. That is, the spanned wire when the processing element (PE) at point A is communicating with PE at point F or spanned wire when PE from point G is communicating with PE at point H. In Figure 1, when the memory controllers and the bridges deliver a bit of a flipped polarity with the previous bit to the interconnect wire (bus), the signal on the bus changes from state "0" to "1" or vice versa as the case may be. Therefore, the lump capacitor charges or discharges thereby consume or dissipates energy accordingly. It should be noted that the modelled wire consumes energy whenever the data traffic flipped state, otherwise consumes no energy. That is, $Pwbit_{0\to0} = Pwbit_{1\to1} = 0$ and $Pwbit_{1\to0} = Pwbit_{0\to1}$ = Energy consumed

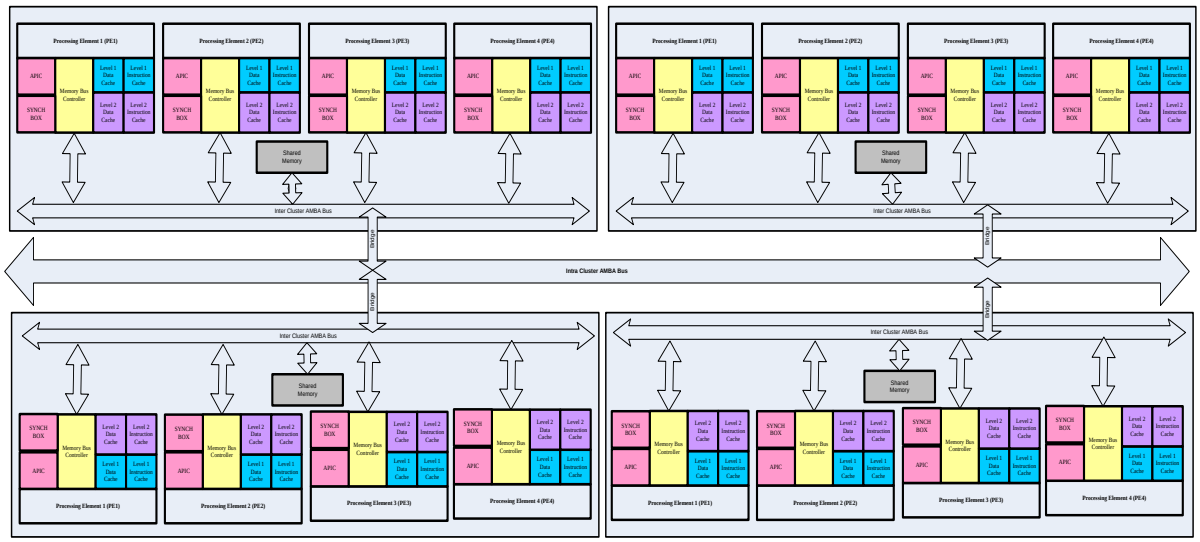

Figure 1 A Hierarchical Shared Bus Based Multiprocessor (HSBSM) [12]

Figure 2 Schematic of a maximum wire span during Processing Elements communication in HSBSM

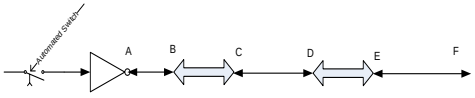

Figure 3 Maximum wire span with 2 bridges in HSBSM

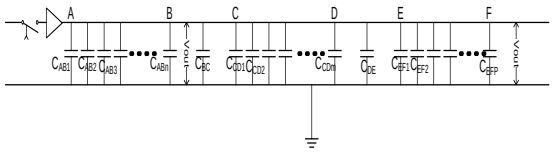

Figure 4Parasitic capacitance model of the maximum spanned wire (AF) with two bridges (C_{BC}& C_{DE}) in HSBSM.

3.1 Wire to Wire Model of HSBSM

The spanned wire for the maximum power consumed in HSBSM occurred on wire length AF. The maximum span wire AF is broken into different segments, as shown in Figure 3, that is AB, BC,CD, DE and EF. Meanwhile segments BC and DE are bridges B_1 and B_2. Figure 4 shows the parasitic capacitance model of the spanned wire (AF) and bridges (C_{BC}&

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C_{DE}). Each of the segments is modelled using their respective lump capacitance.

3.1.1 Model for Wire Length AB and Bridge B1

The circuit equivalent of wire length AB and bridge B1 is shown in Figure 5.

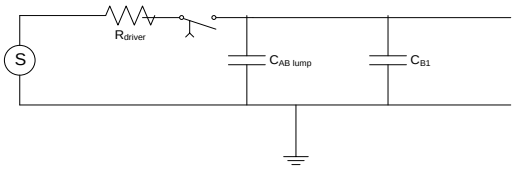

Figure 5 The circuit equivalent of wire AB and bridge B_1

$C_{AB} = C_{ABlump} = C_{AB1}+C_{AB2}+\ldots\ldots\ldots+C_{ABn}$

Total capacitance with bridge = $C_{AB} + C_{B1}$

3.1.2 Model for Wire Length EF and Bridge B2

For wire EF and bridge B2 the equivalent circuit is shown in Figure 6:

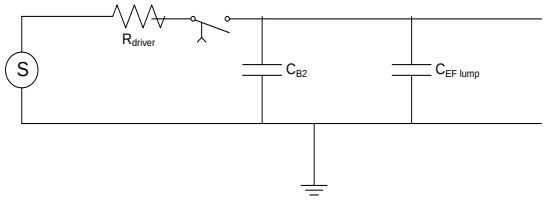

Figure 6 Circuit equivalent of wire EF and bridge B_2

$C_{EF} = C_{EFlump} = C_{EF1}+C_{EF2}+\ldots\ldots\ldots +C_{EFP}$

Total capacitance with bridge = $C_{EF} + C_{B2}$

3.1.3 Model for Wire Length CD

For wire CD the equivalent circuit is shown in Fig.7:

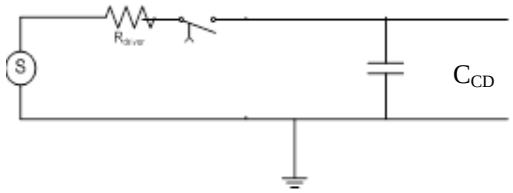

Figure 7 Circuit equivalent of wire C_{CD}

Since the wire is uniform, it is assumed that the wire resistance is uniform and is equal to $R_{w.}$ The R_{driver} is the bus buffer of the shared path, and has a resistance from the root node A to F which is:

$$R_{driver} = \sum RD_j \rightarrow (RD_j \in [path(A \rightarrow B) \cap path(C \rightarrow C) \cap path(C \rightarrow D) \cap path(D \rightarrow E) \cap path(E \rightarrow F)]$$

$$Total\ resistance\ R = R_{driver} + R_w$$

The total resistance $R = R_{driver}$

For an ideal bus

$$R_w \cong 0$$

This implies that the total path resistance is very small and the lump parasitic capacitance of the whole wire is shown in Figure 8.

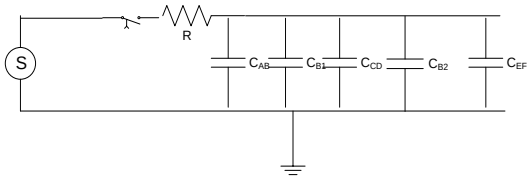

Figure 8 Lump parasitic capacitance model of the maximum spanned wire (AF) and bridges (C_{B1}& C_{B2})

The total lump capacitance of the wire A to F shown in Figure 8 is re-modelled as shown in Figure 9.

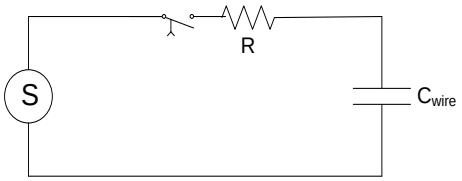

Figure 9 Lump parasitic capacitance model of the maximum spanned wire (AF)

$$C_{wire} = C_{AB} + C_{CD} + C_{EF}$$

Meanwhile the total lump capacitance of the B1 and B2 bridges shown in Figure 7 is:

$$C_{input} = C_{B1} + C_{B2}$$

Therefore, the two bridges in Figure 8 can be modelled as in Figure 10.

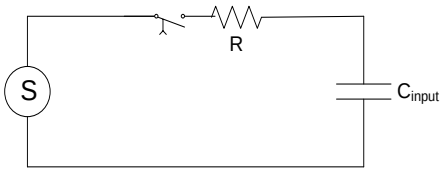

Figure 10 Total lump parasitic capacitance model of bridges

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Wire Bit Energy = ED|C ⊕ EC|C

Where:
$E_{D|C}$ is energy consumed when data bit changes from 1 → 0. $E_{C|C}$ is energy consumed when data bit changes from 0 → 1.

β = Charging rate of the capacitor
$E_{D|C} \approx E_{C|C.}$

$$V_c = E\left(1 - e^{-t/RC}\right) \quad (1)$$

Since,

$$E = V_R + V_c \quad (2)$$

For an ideal multiprocessor interconnection network

$R \cong 0$
$V_c = E\left(1 - e^{-t/0*C}\right)$

$$V_c = E(1 - e^{-\infty})$$
$$e^{-\infty} \cong 0$$

$$\therefore V_c = E \quad (3)$$

Substitute eqn. 4 into eqn.2

$V_C = V_R + V_C$

$V_R = Vc - V_C$

$\Longrightarrow E = V_C = V$

Wire Bit Energy (per unit length) = Energy stored in the lump parasitic capacitor of the wire =
$ED|C = \frac{1}{2} C_{wire} V_{c\,\beta}^2 = \frac{1}{2} C_{wire} V_\beta^2$

Bridge Bit Energy = $ED|C = \frac{1}{2} C_{input} V_{c\,\beta}^2 = \frac{1}{2} C_{input} V_\beta^2$

∴Total Wire Bit Energy for wire length l =

(Wire Bit Energy)* l + 2* Bridge Bit Energy (4)

Max. spanned wire length (l) =

$$2 * W_{inter\ AMBA\ bus} + W_{intra\ AMBA\ bus} + 2 * W_{bridge} + 2 * W_{shared\ memory\ bus} \quad (5)$$

$$WireBitEnergy(P_{wbit}) = \frac{1}{2} C_{wire} V^2\beta + \frac{1}{2} C_{input} V^2\beta \quad (6)$$

where:
$LengthofIntraAMBAbus = W_{intra}$

$Length\ of\ Inter\ AMBA\ bus = W_{inter}$

$Length\ of\ shared\ memory\ bus = W_{shared\ memory\ bus}$

Assuming that both inter and intra AMBA connection wires are uniform then:

$$\text{Max. wire Bit Energy through the HSBSM} = \frac{1}{2} C_{wire} V^2\beta\left((2 * W_{intra\ AMBA} + W_{inter\ AMBA} + 2 * W_{shared\ memory\ bus}) + 2 * Bridgeenergy\right) \quad (7)$$

$$= C_{wire} V^2\beta * W_{intra\ AMBA} + \frac{1}{2} C_{wire} V^2\beta * W_{inter\ AMBA} + C_{wire} V^2\beta * W_{shared\ memory\ bus} + C_{input} V^2\beta \quad (8)$$

For the global wire in 0.18µm technology the wire capacitance is approximately 0.50fF/µm, rail to rail voltage of 3.3V and the activity factor β = 0.5 [13].

These values are used in equation 8 to obtain the estimated wire bit energy of HSBSM shared bus IN. Also several traffics of different sizes were randomly generated for different bus cycles of the hierarchical shared bus of HSBSM.

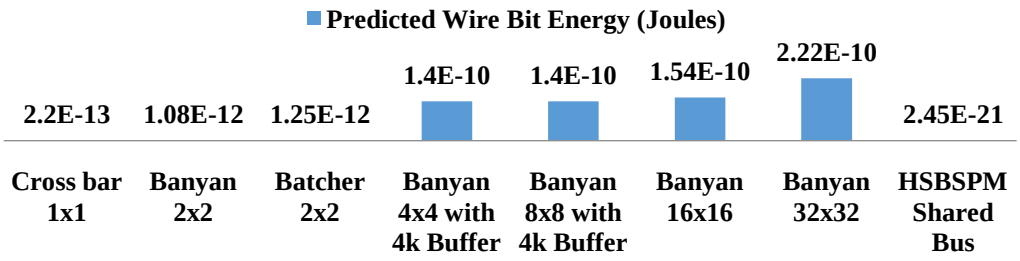

Figure 10 Comparison of Predicted wire bit energy (Pwbit) of the hierarchical Shared Bus with other existing Interconnection Networks

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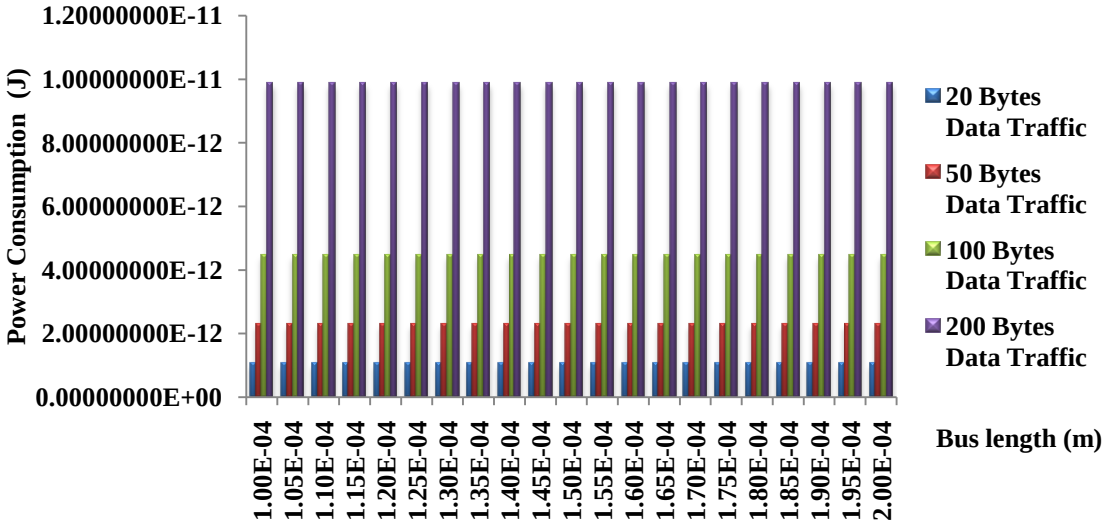

Figure 11 Power Consumption of different data traffics against different Bus lengths

TABLE 1: PREDICTED WIRE BIT ENERGY (*Pwbit*) OF THE HIERARCHICAL SHARED BUS IN AND OTHER INS

S/n	Interconnection Network	No. of switches	Bit Energy 10^{-12} Joule
1	Cross bar 1x1	1	0.22
2	Banyan 2x2	2	1.08
3	Batcher 2x2	2	1.25
4	Banyan 4x4 with 4k Buffer	4	140.00
5	Banyan 8x8 with 4k Buffer	8	140.00
6	Banyan 16x16	16	154.00
7	Banyan 32x32	32	222.00
1	HSBSM Shared Bus	0	$2.45x10^{-21}$

4. RESULTS AND CONCLUSION

From the mathematical model of the wire bit energy shown in equation 8 using per unit minimum bus length and rail-to rail voltage of $0.18\mu m\ and\ 3.3V$ respectively the wire bit energy ($Pwbit$) of 2.45025e-21 J was recorded for the hierarchical shared bus interconnection network. Table 1 and Figure 10 show the predicted wire bit energy ($Pwbit$) of the HSBSM shared bus interconnection network and those of Banyan2x2, Batcher2x2, Banyan4x4 , Banyan 16x16 and Banyan 32x32interconnection networks. The estimated maximum energy consumed for fourrandomly generated data traffics of different sizes, using the energy model in equation 8, for different bus length were obtained and plotted against transmitted bus lengths as shown in Figure 11. Figure 11 pictorially indicates the relationship between the energy consumption of HSBSM for different data traffics at transmission distance interval of $5 * 10^{-6}m$.

The results in Table 1 and Figure 10 indicate that hierarchical shared bus has the lowest wire bit energy compared to other interconnection networks. This implies that any multiprocessor using the hierarchical shared bus will consume lower energy compare to same multiprocessor using any of the evaluated interconnection networks. Also, Figure 11 showed that increased in the size of transmitted data may or may not increase the energy consumption of the multiprocessor using hierarchical shared bus interconnection network, which is energy consumption rate depends on the amount of transitions between 0 to 1 and 1 to 0 in the data. In other word, larger size data with few number of bit transitions consumes less power compare with smaller size data containing more bit transitions during data transfer. That is, apart from bus length another major energy consumption issue is the total number of logic state flipping or transitions in the data traffic. However, irrespective of the size of the data, it is observed that the power consumption of hierarchical shared bus interconnection network increased as the bus length increased.

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