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Design of Low Power Flip Flop Based on Modified GDI Primitive Cells and Its Implementation in Sequential Circuits

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Abstract: *Flip flops are the vital components that act as memory elements in all high performance and low area sequential circuits. This paper aims at proposing a modified gate diffusion input (GDI) based D-flip flop and a novel Universal shift register and 4-bit modulo synchronous counter using Modified gate diffusion input (GDI) techniques. The simulations are performed using tanner electronic design automation (EDA) 13.0 tool using 130nm technology at 1.2V. The result obtained shows increased power delay product and efficient reduction in area among GDI sequential circuits compared to conventional CMOS designs.*

Keyword: *Flip flop; Gate diffusion input; Universal shift register; Counter.*

1. INTRODUCTION

The basic gate diffusion input (GDI) cell looks similar to a complementary metal oxide semiconductor (CMOS) inverter but differs in various functionalities. The GDI cell contains four terminals namely G, P, N and D. The terminal 'P' is the diffusion-node of positive metal oxide semiconductor (PMOS) transistor, terminal 'N' represents the diffusion-node of negative metal oxide semiconductor (NMOS) transistor, the terminal 'G' represents the common gate input terminal of both PMOS and NMOS transistor and the terminal 'D' represents the common diffusion-node of both NMOS and PMOS transistor which acts as output [1]. Fig. 1 shows the structure of basic GDI cell.

The novelty of the design is that both PMOS and NMOS transistors are provided with individual independent inputs to realize more number of logic functions with less transistor count as well as reduced power consumption.

Flip flops are the vital components that act as memory elements in all high performance and low area sequential circuits [2]. Various flip flops are surveyed and analyzed in [3], [4], [5], [6]. This paper aims at proposing a Universal shift register and 4-bit modulo synchronous counter using Modified GDI techniques. The Table I represents the logic functions that can be achieved using GDI cell. All gates can be achieved from F1 and F2 gates hence more concentrated.

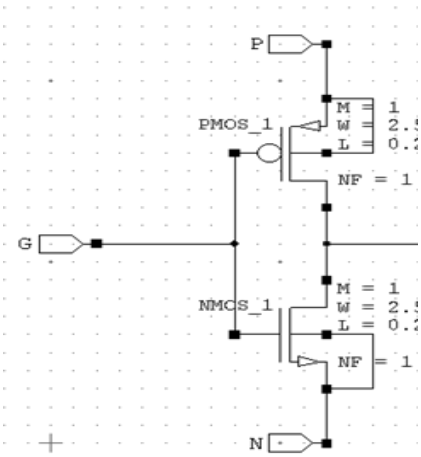

Figure 1 Structure of basic GDI cell

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TABLE I LOGIC FUNCTIONS FROM GDI CELL

N	P	G	D	Function
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B + AC	MUX
0	1	A	A'	NOT

The Primitive cells that are generated from basic GDI cell is represented in Fig. 2 which includes two input AND, two input NAND, three input NAND, two input EX-OR, two input OR and 2 X 1 multiplexer (MUX).

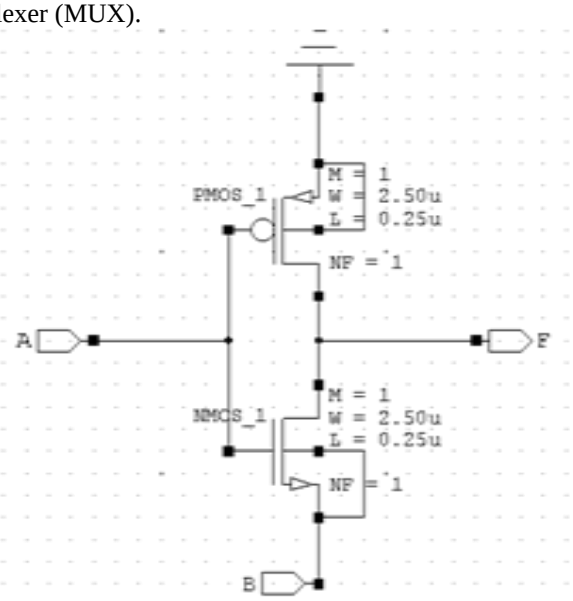

Figure 2(a) 2 Input GDI AND

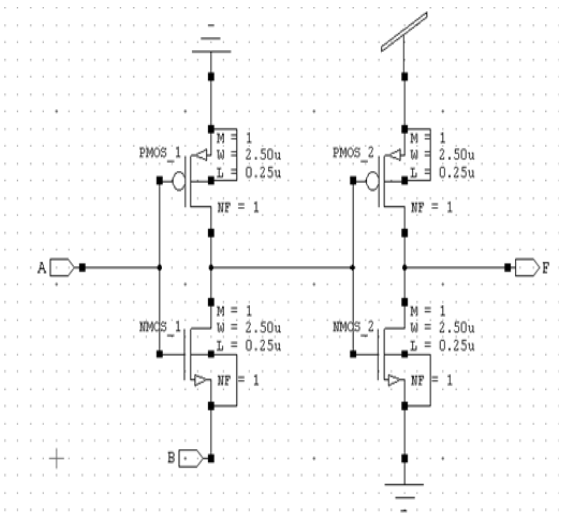

Figure 2(b) 2 Input GDI NAND

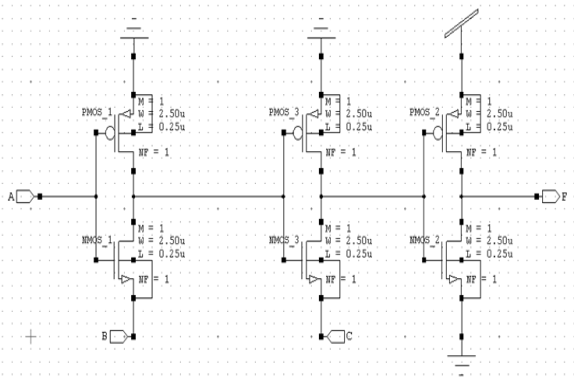

Figure 2(c) 3 Input GDI NAND

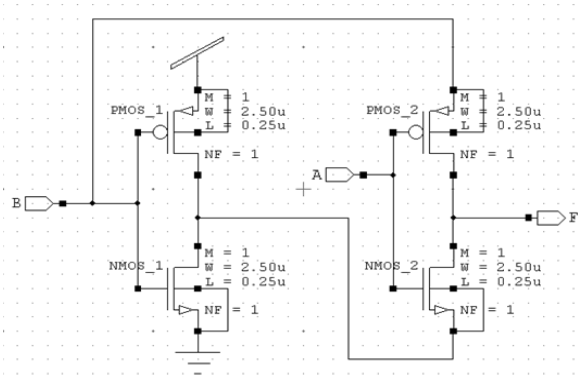

Figure 2(d) 2 Input GDI EXOR

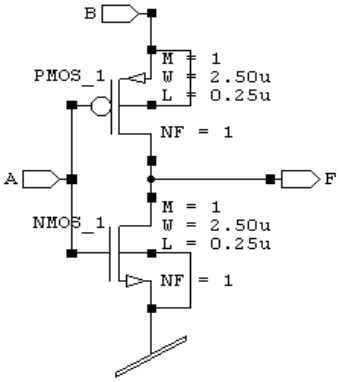

Figure 2(e) 2 Input GDI OR

The major drawback of the GDI primitive cells is that the cost of fabrication is high since it requires twin-well CMOS process [2]. The bulk terminal (diffusion node of both PMOs and NMOs in GDI cell) are not biased properly leading to variations in threshold voltage [7]. The diodes between NMOS and PMOS conducts under condition N=1 and P=0, resulting in reduced output voltage Vout=0.5Vdd. This phenomenon affects the full swing voltage at the output. The structure of the modified GDI primitive cell is represented in Fig. 3

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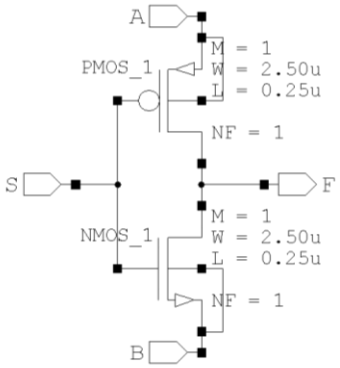

Figure 2(f) 2X 1 GDI Multiplexer

Figure 2(a)-2(f) Primitive Cells of GDI

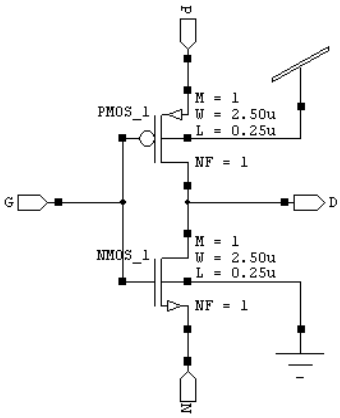

Figure 3 Structure of basic modified GDI cell

The Table II represents the logic functions that can be achieved using GDI cell. The major difference is the continuous Vdd and Gnd to bulk regions of PMOS and NMOS respectively.

TABLE II LOGIC FUNCTIONS FROM MODIFIED GDI CELL

N	P	G	D	Function
0	B	A	A'B	F1
B	1	A	A'+B	F2
A	B	A	A+B	OR
B	A	A	AB	AND
C	B	A	A'B + AC	MUX
0	1	A	A'	NOT

Basic gates required to implement a latch, flip flop, Counter and Universal shift register are achieved using modified GDI cell which includes two input AND, two input NAND, three input NAND, two input OR , two input EX-OR, and 2 X 1 MUX as shown in Fig. 4.

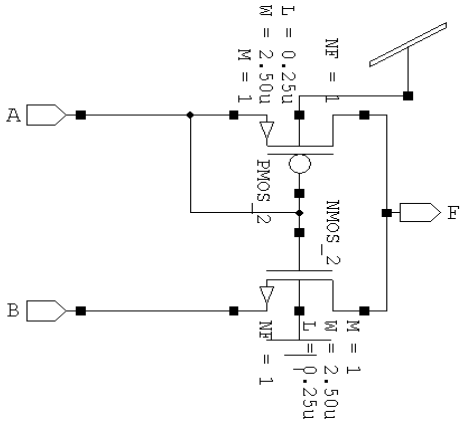

Figure 4(a) 2 Input MGDI AND

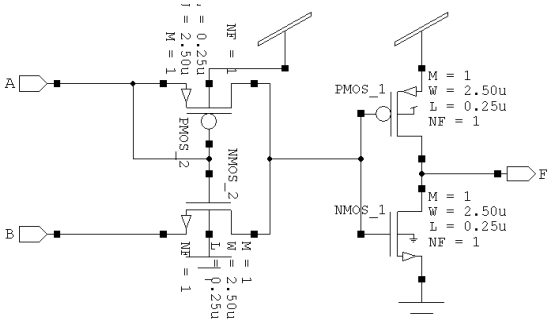

Figure 4(b) 2 Input MGDI NAND

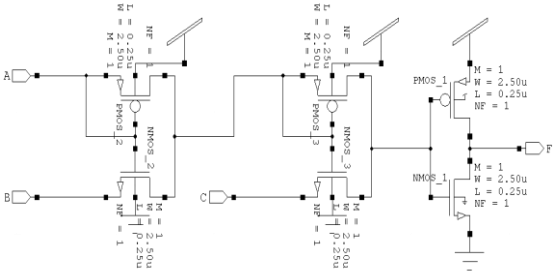

Figure 4(c) 2 Input MGDI NAND

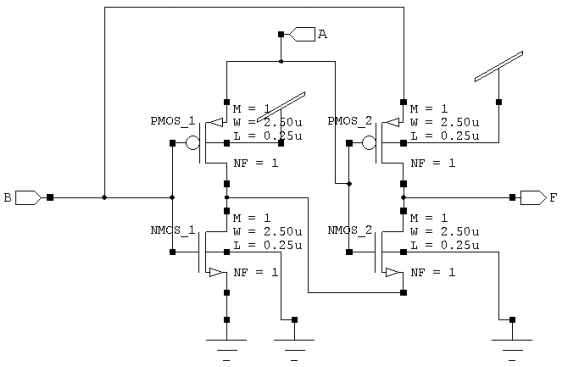

Figure 4(d) 2 Input MGDI EXOR

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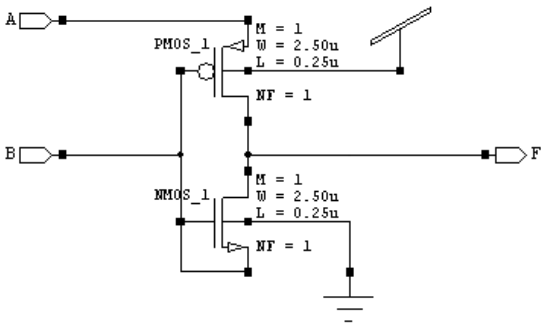

Figure 4(e) 2 Input MGDI OR

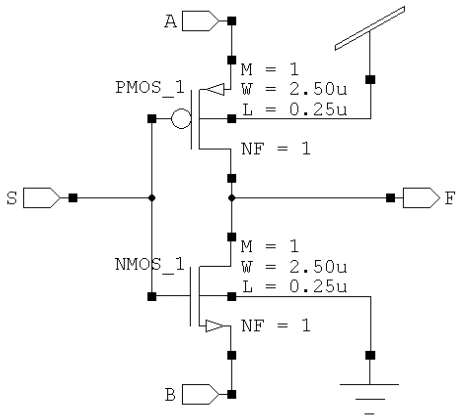

Figure 4(f) 2X 1 MGDI Multiplexer

Figure 4(a)-4(f) Primitive Cells of MGDI

2. RELATED WORK

2.1 MGDI Latch

The design of D-flip flop using GDI logic aims at low design complexity and reduced power consumption [1].

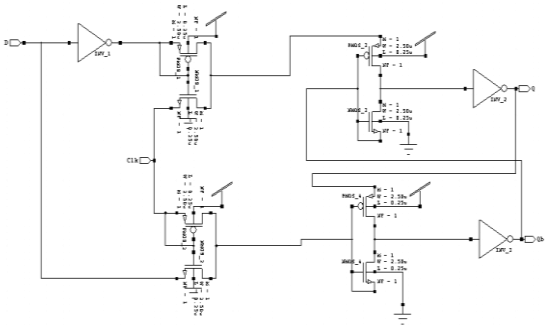

Figure 5 Cross Coupled D-Latch using MGDI AND and NOR gates

This design shows a typical latch based on MGDI logic. However an efficient implementation of D-latch can be achieved by cross coupling MGDI AND and MGDI NOR gates. The structure of the D-latch using MGDI technique is shown in Fig. 5. The data signal 'D' is given to the gate input of AND gate by MGDI cell and drain of the next AND gate by inverting the given data signal. This is responsible for determining the present and next state of the circuit. Both the gates are controlled by the clock signal in order to hold the data at various positive and negative levels. The transmission occurs at diffusion terminal of the GDI cell. The output waveform indicating the operation of MGDI latch is shown in Fig. 6.

Since latches are level triggered, the delay between occurrence of the positive levels or negative levels is greater and finds its implementation in selective architectures.

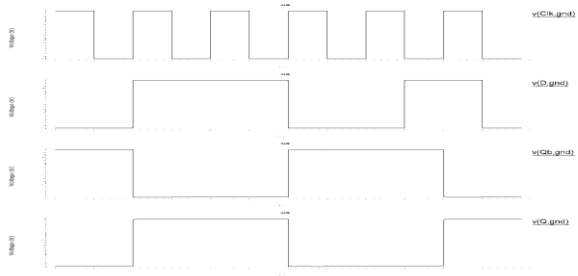

Figure 6 Output waveform of Cross Coupled D-Latch using MGDI AND & NOR gates

The timing analysis and power consumption of MGDI latch is discussed widely in Table IV. Recent day VLSI architectures demand edge triggered flip flops. Hence a MGDI-based positive and negative edge triggered flip flops are designed using basic MGDI gates.

2.2 Positive And Negative Edge Triggered Flip Flops Using MGDI Logic

Edge triggered flip flops normally read the data only at the arrival of positive or negative edges.

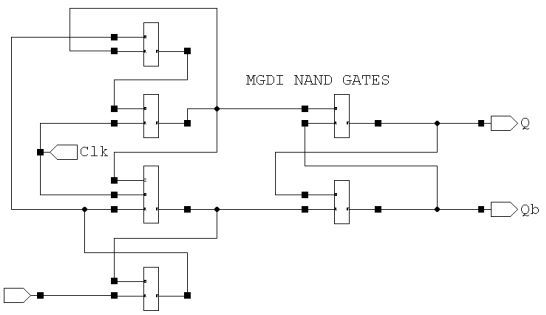

Figure 7 MGDI-based Positive Edge Triggered D Flip Flop

When the data is read and immediately sent to output Q during the clock 0 to 1, then it is said to be positive edge triggered. Similarly when the data is read

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and immediately sent to output Q during the clock 1 to 0, then it is said to be negative edge triggered. The structure of MGDI-based positive edge triggered and negative edge triggered D flip flops are shown in Fig. 7 and Fig. 9 respectively. The design uses 2 input NAND and 3 input NAND primitive cells as shown in Fig. 4(b) and Fig. 4(c). The timing analysis and power consumption of MGDI PETFF is discussed widely in Table IV.

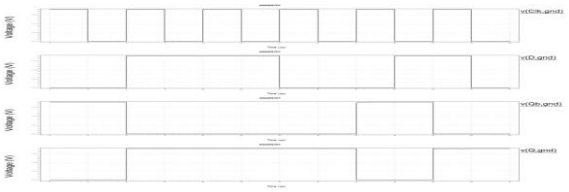

Figure 8 Output waveform of MGDI-based Positive Edge Triggered D Flip Flop

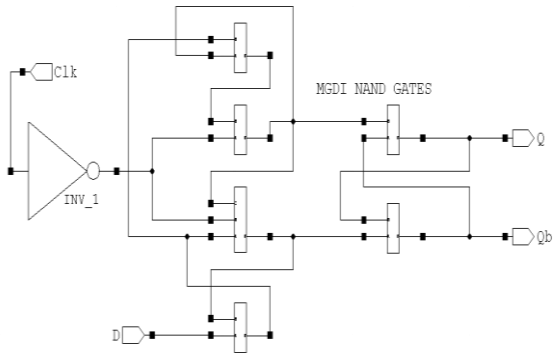

Figure 9 MGDI-based Negative Edge Triggered D Flip Flop

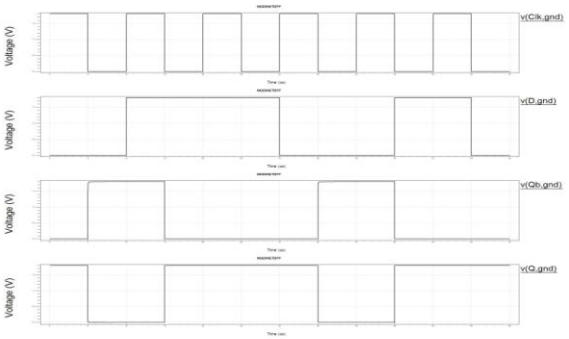

Figure 10 Output waveform of MGDI-based negative Edge Triggered D Flip Flop

The output waveform indicating the operation of MGDI-based Positive and Negative edge Triggered D Flip flop is shown in Fig. 8 and Fig. 10 respectively. Since rising edge is preferred for all sequential circuits [4], a Universal shift register and four bit modulo synchronous counter are implemented using MGDI-based positive edge triggered flip flops.

3. MGDI IMPLEMENTATIONS

3.1 Four Bit Modulo Synchronous Counter Using MGDI-Based Positive Edge Triggered D- Flip Flops

Counters comprising of a number of flip-flops, count a stream of pulses applied to the counter's clock input. The output is a binary value whose value is equal to the number of pulses obtained at the clock input. A counter stores the number of times a event occurred in accordance to a clock signal [5]. The most common type is a sequential digital logic circuit with an input line called the clock and multiple output lines. The number of bits in the counter depends on the pulse applied to the clock input. In digital circuits, Counters are essential component, and are manufactured as separate integrated circuits and also incorporated as parts of larger integrated circuits.

The synchronous counter helps in high-speed operation since clock pulses are given as input to every flip-flop at the same time [4]. An efficient implementation of MGDI-based four bit modulo synchronous counter using MGDI-based positive edge triggered D flip flops is shown in Fig. 11 and its respective waveforms are shown in Fig. 12.

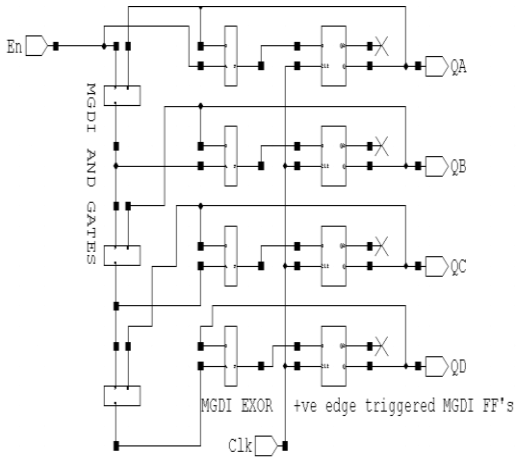

Figure 11 MGDI-based 4-bit Modulo Synchronous Counter using Positive edge triggered MGDI D flip flop

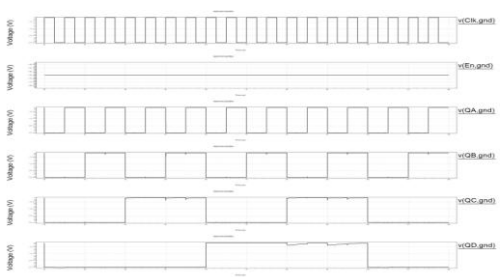

Figure 12 Output Waveform of MGDI-based 4-bit Modulo Synchronous Counter using Positive edge triggered MGDI D flip flop

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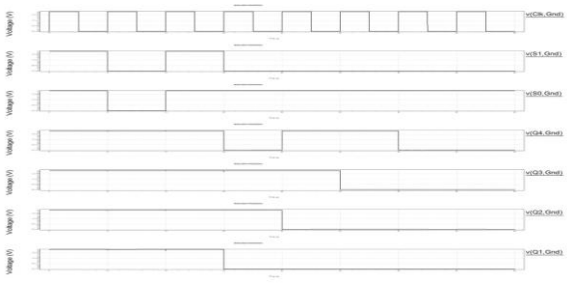

Figure 13 MGDI-based 4-bit Universal Shift Register using Positive edge triggered MGDI D flip flop

3.2 Four Bit Universal Shift Register Using MGDI-Based Positive Edge Triggered D Flip Flops

A universal shift register is a circuit that transfers data in various modes like left shift, right shift, rotate and parallel load [5]. Similar to a parallel register it can load and transmit data simultaneously. Like shift registers it can also load and transmit data in serial fashions through left or right shifts. In addition, the universal shift register combine the capabilities of both parallel and shift registers. On a particular job, a universal register can load data in series and then transmit output data in Parallel [6]. Universal shift registers are also used in computers as memory elements. The different modes of operation in universal shift register in the block diagram are shown as follows.

TABLE III OPERATING MODES OF UNIVERSAL SHIFT REGISTER

Operating Mode	S1	S0
Lock	0	0
Right Shift	0	1
Left Shift	1	0
Parallel load	1	1

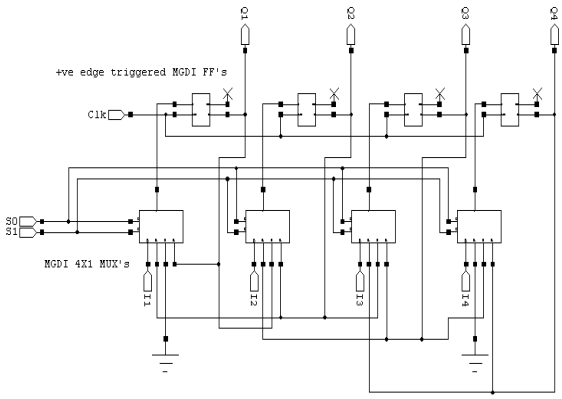

Figure 14 MGDI-based 4-bit Universal Shift Register using Positive edge triggered MGDI D flip flop- Right Shift

The structure of four bit Universal Shift Register using MGDI-based Positive Edge triggered D flip flops is shown in Fig. 13 .The waveforms showing right shift and left shift operation are shown in Fig. 14 and Fig. 15 respectively.

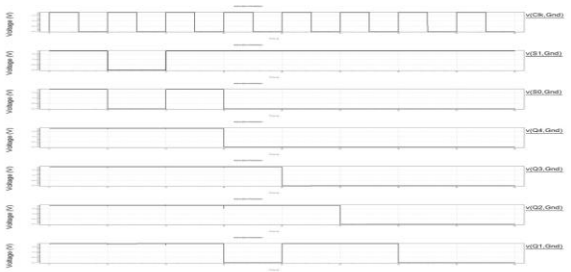

Figure 15 MGDI-based 4-bit Universal Shift Register using Positive edge triggered MGDI D flip flop-Left Shift

3.3 Positive and Negative Edge Triggered D Flip Flops Using MGDI Multiplexer

The design of positive and negative edge triggered flip flops can also be designed using MGDI multiplexer. The design representing positive and negative triggered flip flops using multiplexer is shown in Fig. 16(a) and Fig. 16(b) respectively.

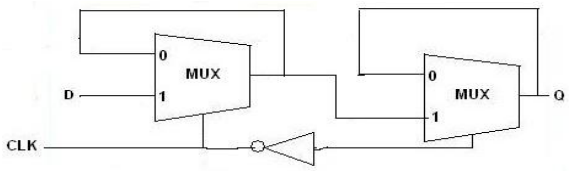

Figure 16(a) Structure of Positive Edge Triggered D Flip Flop using MUX

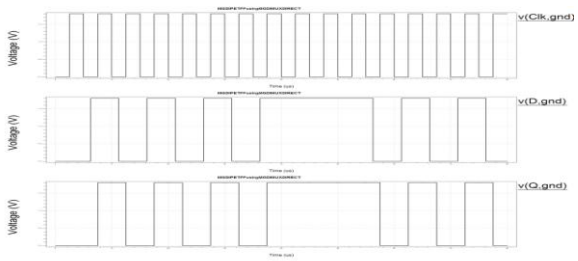

Figure 16(b) Structure of Negative Edge Triggered D Flip Flop using MUX

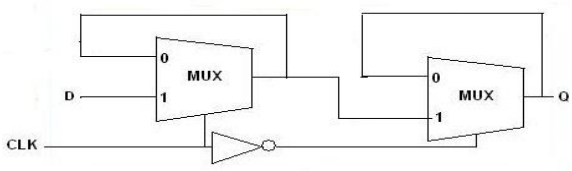

Figure 17(b) Structure of Negative Edge Triggered D Flip Flop using MGDI MUX

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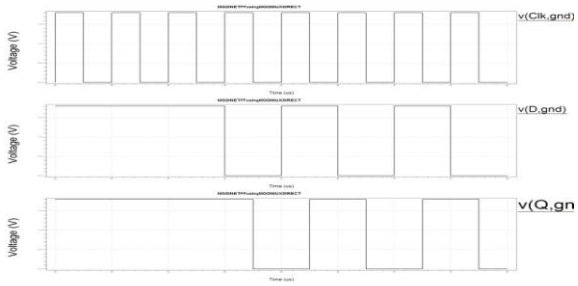

Figure 18 Output waveform of Positive Edge Triggered D Flip Flop using MGDI MUX

The design of MGDI-based multiplexer is shown in Fig. 2.4(f). The input A and B are connected to P and N terminal of the MGDI cell. The selection line is connected to the gates of both PMOS and NMOS transistor. The selection input decides the corresponding inputs to propagate through the output. The MGDI multiplexer consumes less number of transistor compared to conventional CMOS multiplexers. Reduced power consumption and effective decrease in area of MGDI multiplexer finds its advantage in the design of positive and negative edge triggered flip flops.

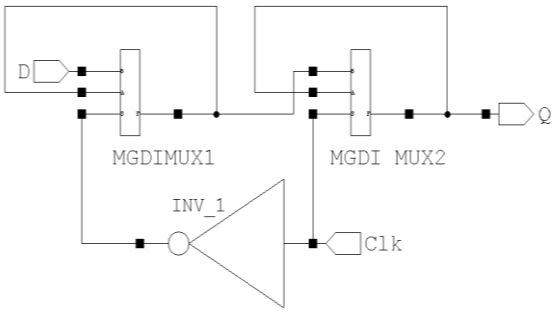

Figure 17(a) Structure of Positive Edge Triggered D Flip Flop using MGDI MUX

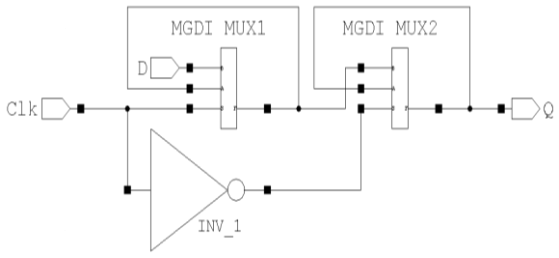

Figure 19 Output waveform of Negative Edge Triggered D Flip Flop using MGDI MUX

Hence the design of MGDI MUX based positive and negative edge triggered flip flops can be obtained by implementing the MGDI MUX in the structure represented in Fig. 16(a) and Fig. 16(b). The design showing the positive and negative edge triggered flip flops based on MGDI MUX is shown in Fig. 17(a) and Fig. 17(b) respectively. The output waveforms of the proposed structure is shown in Fig. 18 and Fig. 19.

3.4 Design of 4-Bit Modulo Synchronous Counter and Universal Shift Register with Positive Edge Triggered D Flip Flops Using MGDI Multiplexer

The number of transistors is considerably low while designing the edge triggered flip flops based on MGDI multiplexer which leads to reduced power consumption and efficient area reduction.

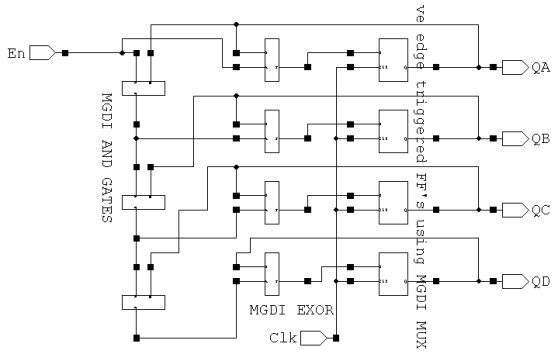

Figure 20 MGDI-based 4-bit Modulo Synchronous Counter with Positive edge triggered D flip flop using MGDI multiplexer

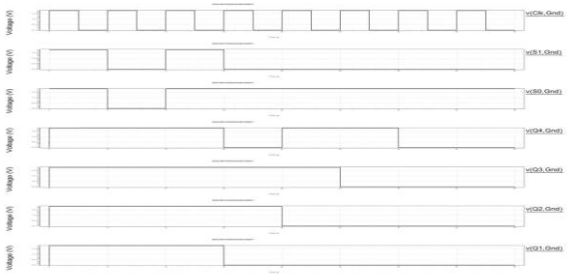

Figure 21 MGDI-based 4-bit Universal Shift register with Positive edge triggered D flip flop using MGDI multiplexer

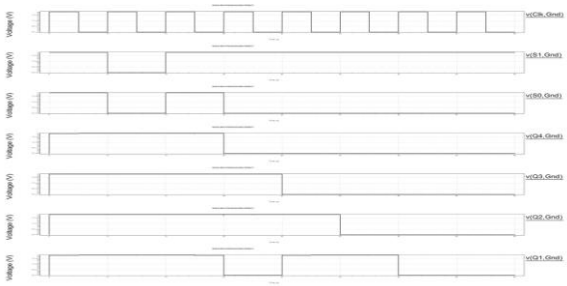

Figure 22 Output waveform of MGDI-based 4-bit Modulo Synchronous Counter with Positive edge triggered D flip flop using MGDI multiplexer

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Hence the design of 4 bit modulo synchronous counter and Universal shift register with positive edge triggered D flip flops using MGDI multiplexer is done. The timing analysis and power consumption of these designs are discussed widely in Table IV. The design of 4 bit modulo synchronous counter and Universal shift register with positive edge triggered D flip flops using MGDI multiplexer is represented in Fig. 20 and Fig. 21 respectively.

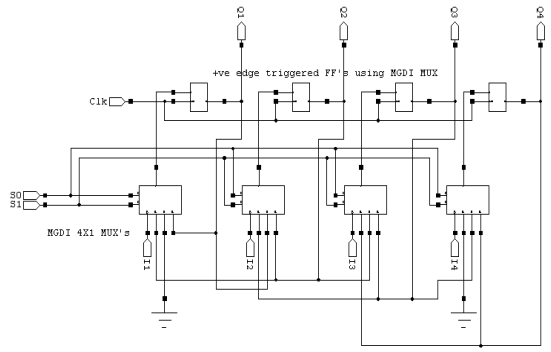

Figure 23(a) Output waveform of MGDI-based 4-bit Universal Shift register with Positive edge triggered D flip flop using MGDI multiplexer-Shift right

The output waveforms of 4 bit modulo synchronous counter and Universal shift register with positive edge triggered D flip flops using MGDI multiplexer is represented in Fig. 22 and Fig. 23(a) and Fig. 23(b) respectively.

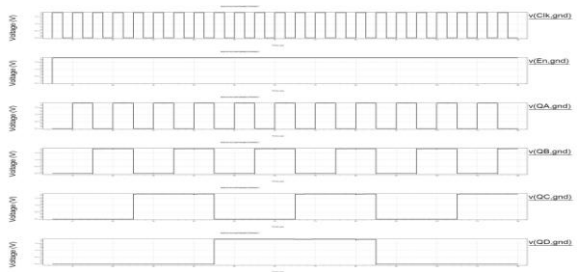

Figure 23(b) Output waveform of MGDI-based 4-bit Universal Shift register with Positive edge triggered D flip flop using MGDI multiplexer-Shift left

3.5 Dual Edge Triggered Flip Flops

Certain sequential circuits require dual edge triggered flip flops for their operation. The structure of dual edge triggered flip flops is shown in Fig. 24.

Dual edge triggered flip flops are designed using two ways:

(a) Dual edge triggered flip flop using positive and negative triggered MGDI flip flops connected to a MGDI multiplexer. When Clock is zero, positive edge triggered flip flop is selected to output and when clock is one, negative edge triggered flip flop is connected to output. The design of Dual edge triggered flip flop using positive and negative triggered MGDI flip flops is shown in Fig. 25.

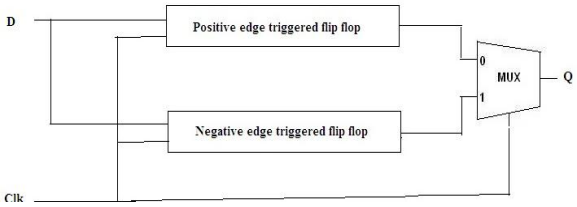

Figure 24 Structure of dual edge triggered flip flop

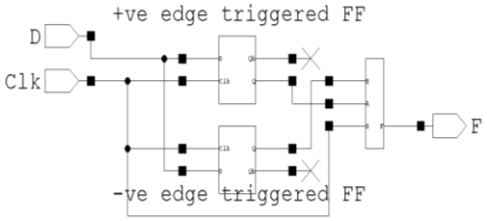

Figure 25 Dual edge triggered flip flop using positive and negative triggered MGDI flip flops

The output waveform of Dual edge triggered flip flop using positive and negative triggered MGDI flip flops is shown in Fig. 26.

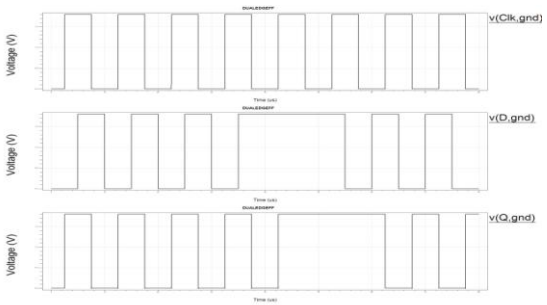

Figure 26 Output waveform of Dual edge triggered flip flop using positive and negative triggered MGDI flip flops

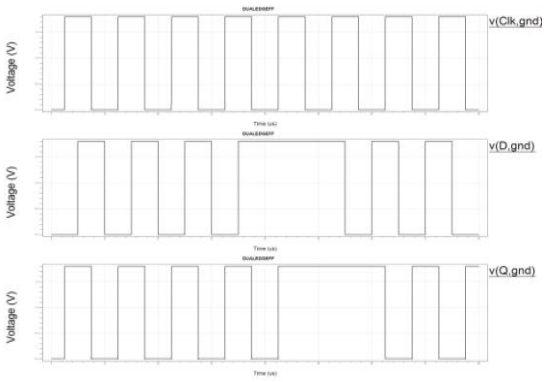

Figure 27 Output waveform of Dual edge triggered flip flop with positive and negative triggered MGDI flip flops using MGDI MUX

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(b) Dual edge triggered flip flop with positive and negative triggered MGDI flip flops using MGDI MUX connected to a MGDI multiplexer. The design comprises of five MGDI multiplexers which consumes less number of transistor than the previous design. This design is achieved by introducing positive and negative edge triggered MGDI flip flops using MGDI multiplexer in Fig. 25. The output waveform of Dual edge triggered flip flop with positive and negative triggered MGDI flip flops using MGDI multiplexer is shown in Fig. 27.

4. SIMULATION RESULTS & ANALYSIS

The proposed designs such as MGDI-based D-latch, MGDI-based Positive and Negative Edge Triggered D Flip Flop, MGDI-based 4-bit Modulo Synchronous Counter using Positive edge triggered MGDI D flip flop, MGDI-based 4-bit Universal shift register using Positive edge triggered MGDI D flip flop, Positive and Negative edge Triggered D Flip Flop using MGDI MUX, MGDI-based 4-bit Modulo Synchronous Counter with Positive edge triggered D flip flop using MGDI multiplexer, MGDI-based 4-bit Universal Shift Register with Positive edge triggered D flip flop using MGDI multiplexer, Dual edge triggered flip flop using positive and negative triggered MGDI flip flops and Dual edge triggered flip flop with positive and negative triggered MGDI flip flops using MGDI MUX are simulated using tanner 13.1 EDA 130nm CMOS technology with 1.2 V under nominal operating conditions. The simulation results are tabulated in Table IV. The simulation results indicate reduced power consumption and area than recent logic gates including multifunction reversible logic gates [7].

TABLE IV SIMULATION RESULTS OF VARIOUS MGDI SEQUENTIAL CIRCUITS

GDI Implementations	Total Number of Transistors Used	Total No of clocked Transistors	Average Power Consumption (µW)	Ck to Q Delay (ns)	D to Q delay (ns)	Power delay product (fJ)	Area (µm2)	Static power Consumption (nW)	Dynamic Power Consumption (mW)
MGDI-based D-latch	14	2	0.51	1.8	0.20	0.10	8.75	3.81	0.2
MGDI-based Positive Edge Triggered D Flip Flop	26	2	4.56	0.42	0.6	2.73	16.25	6.57	1.79
MGDI-based Negative Edge Triggered D Flip Flop	28	2	3.83	0.68	0.59	2.25	17.5	7.87	1.42
MGDI-based 4-bit Modulo Synchronous Counter using Positive edge triggered MGDI D flip flop	126	8	41.20	0.51	NA	21.01	78.75	18.32	4.52
MGDI-based 4-bit Universal shift register using Positive edge triggered MGDI D flip flop	128	8	140.26	0.43	0.52	72.93	80	21.26	6.72
Positive/Negative edge Triggered D Flip Flop using MGDI MUX	6	6	2.14	0.25	0.25	0.53	3.75	3.7	0.45
MGDI-based 4-bit Modulo Synchronous Counter with Positive edge triggered D flip flop using MGDI multiplexer	46	24	15.04	0.45	NA	6.76	28.75	1.4	2.6

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MGDI-based 4-bit Universal Shift Register with Positive edge triggered D flip flop using MGDI multiplexer	48	24	52.59	0.47	0.54	28.39	30	10.26	2.82
Dual edge triggered flip flop using positive and negative triggered MGDI flip flops	56	6	5.57	2.42	1.92	10.69	35	5.23	1.52
Dual edge triggered flip flop with positive and negative triggered MGDI flip flops using MGDI MUX	14	14	2.36	1.23	0.84	1.98	8.75	7.5	0.66

Power, area and delay analysis of various modified GDI based flip flops and its implementation in four bit synchronous counter and Universal shift register are performed using TANNER EDA 13.0 with 130nm CMOS technology. The results are represented as pictorial representation for comparative analysis in Fig. 28 and Fig. 29.

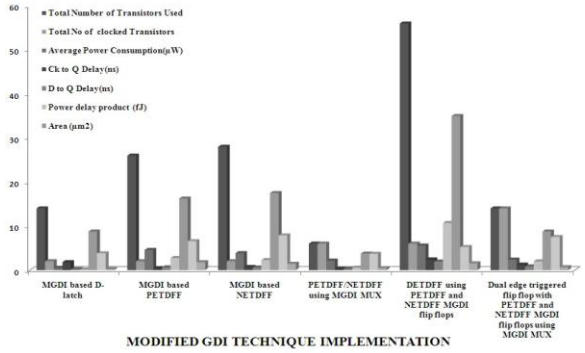

Figure 28 Comparative analysis of various MGDI-based Flip flops

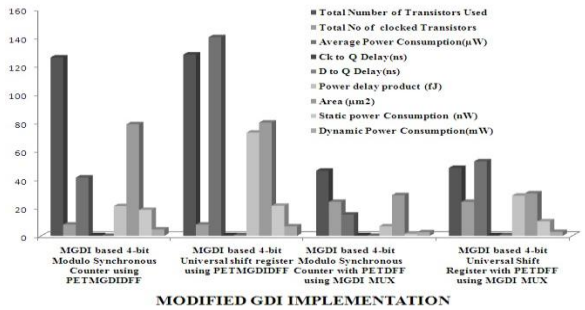

Figure 29 Comparative analysis of various MGDI-based Flip flops implanted in Counter and USR

5. CONCLUSION

GDI based primitive cells are designed and their drawbacks are overcome by modified GDI primitive cells [2]. Various designs using MGDI flip flops and MGDI MUX are proposed and simulated using tanner 13.1 EDA 130nm CMOS technology with 1.2V under nominal operating conditions. The result shows reduced power, area and PDP for MGDI-based flip flops designed using MGDI multiplexer. In future these counter and universal shift register can be implemented in various architectures due to its precise area and power requirements.

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