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A Comparative Study on Electrical Characteristics of MOS ($Si_{0.5}Ge_{0.5}$) and MOS (4H-SiC) Transistors in 130nm Technology with BSIM3v3 Model

Mourad Hebali

Research Scholar, Department of Electrical Engineering, ENP Oran,
Laboratory CaSiCCe, 31000 Oran, Algeria
Email: hebalimourad@yahoo.fr

Djilali Berbara

Research Scholar, Department of Electrical Engineering, ENP Oran,
Laboratory CaSiCCe, 31000 Oran, Algeria
Email: berbara_enset@yahoo.fr

Pr. Mohammed Benzohra

Professor, Department of Networking and Telecommunications, University of Rouen,
Laboratory LECAP, 7600, France
Email: mohamed.benzohra@univ-rouen.fr

Pr. Djilali Chalabi, Pr. Abdelkader Saïdane

Professors, Department of Electrical Engineering, ENP Oran,
Laboratory CaSiCCe, 31000 Oran, Algeria
Email: dchalabi@yahoo.fr, saidaneaek@yahoo.com

Abstract: *Silicon-Germanium is of signicant importance with the introduction of strained layers and SiGe channels into complementary metal-oxide semiconductor (CMOS) technology, and the silicon carbide (SiC) is a very interesting semiconductor for applications in high temperature, high frequency and high power. In this article, we have studied and compared MOS transistors with 130nm $Si_{0.5}Ge_{0.5}$ and 4H-SiC technologies using BSIM3v3 model. To perform this work we have used PSpice to study the I-V characteristics ($I_D=f(V_{DS})$, $I_D=f(V_{GS})$ and I_{ON}/I_{OFF} ratio) and the transconductance g_m as a function of temperature in the range -200°C to 200 °C for MOS$i_{0.5}Ge_{0.5}$ transistor and range -200 °C to 600 °C for MO(4H-SiC) transistor with a supply voltage V_{DS} = 1.2V. We have also calculated the RF characteristics (f_T and f_{MAX}) of the two types of transistors. This comparison demonstrates: the superiority of $Si_{0.5}Ge_{0.5}$ technology in RF characteristics, and superiority of 4H-SiC technology in high I_{ON}/I_{OFF} ratio and high operating temperature, and the MOS$i_{0.5}Ge_{0.5}$ and MO(4H-SiC) transistors operate under a low voltage less than 1.2V and low power in submicron technology.*

Keyword: *$Si_{0.5}G_{0.5}$, 4H-SiC, MOSFET, BSIM3v3, I-V characteristics, RF characteristics.*

1. INTRODUCTION

In 1948, Bardeen, Brattaint and Schockley invented the bipolar transistor. Although the material used was Silicon and Germanium that took over just a few years later in electronics developments. The transition period, which followed around 1960, favored the first studies on the mixing of these two $Si_{1-x}Ge_x$ alloy compounds [1]. Silicon-Germanium is a lower band-gap semiconductor, higher intrinsic carrier concentration, and is one of the materials that have good thermoelectric properties. Used SiGe technology as the high mobility layers in the channel for MOSFET devices for increased device performance without the need for expensive conventional scaling strategies. Furthermore, combining the SiGe system and scaled MOSFET technologies has been shown to offer additional performance gains [2].

In addition to this technology the silicon carbide (SiC) is a wide bandgap semiconductor. It has a high breakdown field, a high saturation velocity of electrons and a high thermal conductivity [3]. This

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semiconductor is generally used to manufacture electronic components which support high voltages and powers [4]. But, we have shown that the MOS transistors in silicon carbide submicron technology work well in low voltage and low power [5]. It grows in many different polytypes, but the most studied are the 3C, 4H, and 6H-SiC [6-7].

From the different parameters of these semiconductors at room temperature which are presented in Table I. In our work, we will use BSIM3v3 as a model for our $MOSi_{0.5}Ge_{0.5}$ and MOS(4H-SiC) transistors, to study and compare the different characteristics of these transistors. Based on the equations of this model [8-9], we will calculate our components, then simulate their characteristics $I_D=f(V_{DS})$, the transfer $I_D=f(V_{GS})$, I_{ON}/I_{OFF} ratio and transconductance $g_m=f(T)$. Our work will be carried for 130nm channel length, 1.2V supply voltage and temperatures between -200°C and 600°C. We will use the small signal equivalent circuit for a MOSFET, to determine the RF (Radio-Frequency) characteristics f_T (Cut-off frequency) and f_{MAX} (maximum oscillation frequency) of different devices.

TABLE I BASIC PARAMETERS OF $Si_{0.5}Ge_{0.5}$ AND 4H-SiC.

Materials / Parameters	$Si_{0.5}Ge_{0.5}$	4H-SiC
Eg (ev) Energy gap	0.8	3.36
μe (cm^2/Vs) Electron mobility μh (cm^2/Vs) hole mobility	167 136	1000-1140 115
n_i (cm^{-3}) Intrinsic carrier concentration	$1{,}2.10^{13}$	$8{,}2.10^{-9}$
Dielectric permittivity (ε)	13,90	6.63
$v_{sat}.10^7$ (cm/s)	1	2
Thermal conductivity $\mathcal{K}$ ($W\,m^{-1}K^{-1}$)	0,088	4.9

2. SIMULATION DETAILS

For our work, we will use the structure of MOS transistors in $Si_{0.5}Ge_{0.5}$ and 4H-SiC technologies of Figure .1 to perform the calculations in order to establish the model and do the simulation.

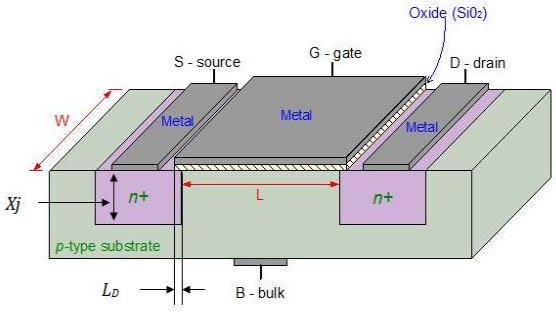

Figure 1 Structure used of MOS($Si_{0.5}Ge_{0.5}$ and 4H-SiC) transistors.

The transistors are identical from the point of view of constitution. They differ only in the nature of the semiconductor material. The doping of the source, the drain and the gate is of the order of $10^{20}cm^{-3}$ for the two transistors. That of the Nch channel, it is equal to $2{,}3549.10^{17}cm^{-3}$ [10]. The doping of substrates N_{sub} is equal to $6.10^{16}cm^{-3}$. In our study, we opted for limiting dimensions allowed by the BSIM3v3 model of the MOSFET transistor [11] (length of the channel L=130nm and its width W=160nm). To realize the 130nm technology, it is necessary to use an oxide layer of thickness Tox=2.3nm, and a polarization of a value V_{DD} = 1.2V [12]. For the PSpice simulation of the BSIM3v3 MOS transistor, we will use level 7 [13].

3. SIMULATION RESULTS AND DISCUSSION

3.1 I-V Characteristics

Figure 2 shows the evolution of I_D drain current as a function of V_{DS} drain voltage of the MOS transistors in (SiGe and 4H-SiC) technology, with gate voltage V_{GS}=1.2V, and at room temperature.

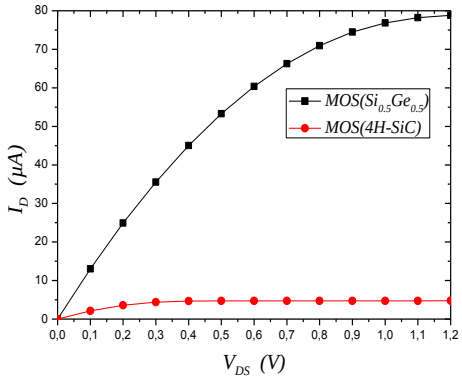

Figure 2 Output characteristic $I_D=f(V_{DS})$ of MOS(SiGe and 4H-SiC) transistors.

The $MOSi_{0.5}Ge_{0.5}$ transistor is characterized by a saturation current 16 times greater than that of transistor in 4H-SiC technology. This is what shows that the MO(4H-SiC) transistor is characterized by a very low power compared to the transistor in $Si_{0.5}Ge_{0.5}$ technology as shown in Figure 1. For BSIM3v3 model the drain current in a point y to this characteristic can be expressed as [8-9]:

$$I_{DS} = \frac{\mu_{eff} C_{ox} W E_{sat}}{E_{sat} L + V_{DS}} \left(V_{gs} - \frac{A_{bulk} V_{DS}}{2} - V_{th} \right) V_{DS} = a\,(b - V_{th})\,V_{DS} \quad (1)$$

where μ_{eff} is the effective mobility, C_{ox} is the oxide capacitor, E_{sat} is the saturation field, V_{th} is the threshold voltage and A_{bulk} is the parameter of BSIM3v3 model.

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The different dimensions of the structure and the type of oxide are the same for these transistors. The parameters *a* and *b* are approximately the same for different transistors. The large variation of the threshold voltage between $MOSi_{0.5}Ge_{0.5}$ and MO(4H-SiC) transistors ($V_{th(Si0.5G0.5)} < V_{th(4H-SiC)}$) causes a huge change in the drain currents of these transistors. The threshold voltage is the responsible on the evolution of the output characteristics.

Figure 3 shows the transfer characteristics for $MOSi_{0.5}Ge_{0.5}$ and MO(4H-SiC) transistors with drain voltage V_{DS}=1.2V.

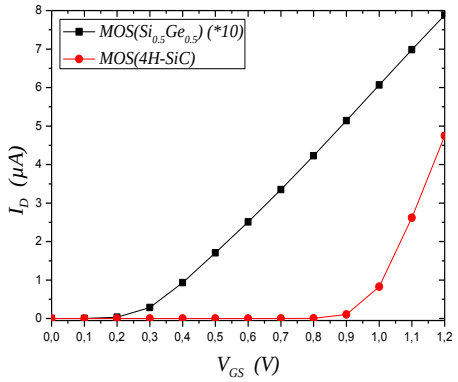

Figure 3 Transfer characteristic $I_D = f(V_{GS})$ of the MOS(SiGe and 4H-SiC) transistors.

This characteristic has been exploited to find the threshold voltages. The parameters which influence the evolution of threshold voltage of the different MOS transistors by considering BSIM3v3 model (Equation 1) are: the carrier mobility ***μ*** and the gap ***Eg*** of each semiconductor. So that the threshold voltage is directly proportional to these parameters. This is what makes the MOS(4H-SiC) transistor is characterized by a high value of threshold voltage compared to MOS(SiGe) transistor as shown in Figure 3.

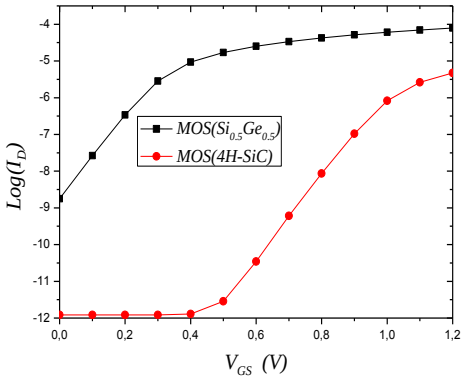

Figure 4 I_{ON} and I_{OFF} of $MOSi_{0.5}Ge_{0.5}$ and MO(4H-SiC) transistors

Figure 4 shows the evolution of *Log(I_D)* as a function of Gate-Source voltage at V_{DD}=1.2V in room temperature. This figure is exploited in order to find I_{ON} and I_{OFF} currents.

The leakage current I_{OFF} of MOS(4H-SiC) transistor is very low compared to the transistor in $Si_{0.5}Ge_{0.5}$ technology as shown in the Figure 4. These results show that the transistor in 4H-SiC technology is characterized by a high I_{ON}/I_{OFF} ratio compared to the $MOSi_{0.5}Ge_{0.5}$ transistor (Table II). The intrinsic carrier concentration *ni* of 4H-SiC is extremely low compared to that of $Si_{0.5}Ge_{0.5}$ (Table I), because of the large gap of this semiconductor. It is an important parameter which conditions for a large part the intensity of the leakage currents of MOS transistors [14].

The MOS transistors operate in sub-threshold regime, to get the leakage current. The drain current expression is written in this regime [8-9]:

$$I_D = \frac{W}{L}\mu_{eff}C_{ox}(\eta-1){V_T}^2\, exp\left(\frac{V_{GS}-V_{Th}}{\eta V_T}\right)\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (2)$$

In the model, the I_{ON} current and leakage current I_{OFF} are defined by the following relationships:

$$I_{ON} = I_D|V_{GS} = V_{DD}, V_{DS} = V_{DD}, V_{bs} = 0 \quad (3)$$

$$I_{OFF} = I_D|V_{GS} = 0, V_{DS} = V_{DD}, V_{bs} = 0 \quad (4)$$

So

$$I_{ON} = \frac{W}{L}\mu_{eff}C_{ox}(\eta-1){V_T}^2\, exp\left(\frac{V_{DD}-V_{Th}}{\eta V_T}\right)\left(1 - exp\left(-\frac{V_{DD}}{V_T}\right)\right) \quad (5)$$

$$I_{OFF} = \frac{W}{L}\mu_{eff}C_{ox}(\eta-1){V_T}^2\, exp\left(\frac{-V_{Th}}{\eta V_T}\right)\left(1 - exp\left(-\frac{V_{DD}}{V_T}\right)\right) \quad (6)$$

The I_{ON}/I_{OFF} ratio of the BSIM3v3 is defined by:

$$\frac{I_{ON}}{I_{OFF}} = \exp\left(\frac{V_{DD}}{\eta V_T}\right) \quad (7)$$

The supply voltage V_{DD} and thermal voltage V_T used is the same for our transistors. Hence, the I_{ON}/I_{OFF} ratio is proportional to the η sub-threshold parameter.

3.2 Transconductance g_m(T) characteristics

Figure 4 shows the evolution of transconductance as a function of temperature in the range -200°C to 200°C and range -200°C to 600°C for $MOSi_{0.5}Ge_{0.5}$ and MO(4H-SiC) transistors respectively. From the drain relation of BSIM3v3 model in saturation region

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and following a simplification, expression of transconductance can be written [5]:

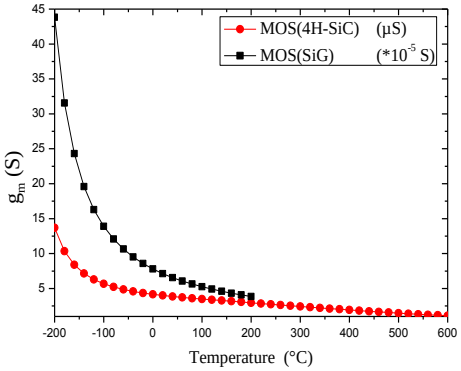

Figure 5 Transconductance of MOSi$_{0.5}$Ge$_{0.5}$ and MO(4H-SiC) transistors.

$$g_m(T) = WC_{ox}v_{sat}(T) = \frac{1}{2}WC_{ox}E_{eff}\mu_{eff}(T) \quad (8)$$

The saturation velocity and carrier mobility are decreased as a function of temperature [8] and so it follows that leads to a reduction in the transconductance $\boldsymbol{g_m}$ whenever the temperature increases as shown in Figure 5. The Thermal conductivity of 4H-SiC is extremely high compared to that of Si$_{0.5}$Ge$_{0.5}$ (Table I). This makes the transistor in 4H-SiC technology work well in a wide range of temperature compared with MOSi$_{0.5}$Ge$_{0.5}$ transistor.

3.3 RF characteristics

The small signal equivalent circuit (Figure 6) of the nMOS transistor is used in the RF characteristics analysis [15], which facilitates the calculation of frequencies f_T and f_{MAX} of these transistors.

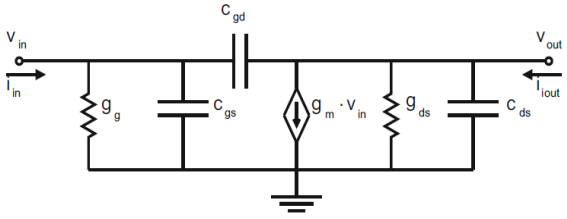

Figure 6 MOS transistor small-signal circuit model.

The cut-off frequency (f_T) expression of MOS transistors is [16-17]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (9)$$

with g_m Transconductance in saturation mode, C$_{gs}$ and C$_{gd}$: Gate-Source and Gate- Drain capacity . They are given by equations (11) and (12).

$$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox} \quad (10)$$

$$C_{gd} = WL_{ov}C_{ox} \quad (11)$$

With $L_{ov} = \frac{C_{gdo}}{C_{ox}}$ where C$_{gdo}$ is PSpice parameter of BSIM3v3 model.

The maximum frequency of oscillation (f_{MAX}) can be expressed as [18]:

$$f_{MAX} = \frac{f_T}{2\sqrt{g_m(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \quad (12)$$

where *Rg* is the gate resistance, *Rs* is the source resistance. There is a geometric symmetry for our devices. So *Rg* = *Rs* = *R*.

$$f_{MAX} = \frac{f_T}{2\sqrt{(g_m + \pi f_T C_{gd})2R}} \quad (13)$$

The expression $2\pi(C_{gs} + C_{gd})$ depends only on transistor dimensions and oxide capacitor C$_{ox}$. Its value is the same for our transistors. Thus, the cut-off frequency is directly proportional to transconductance of these transistors. That's what makes the MOSi$_{0.5}$Ge$_{0.5}$ transistor is characterized by high cut-off frequency compared with MOS transistor in 4H-SiC technology as shown in Table II. The f_{MAX} is a good performance indicator of MOS transistors, so that it includes the effects of gate and source resistances; therefore, its value is less than the f_T value. The results showed that the MOSi$_{0.5}$Ge$_{0.5}$ transistor characterized by high performance in RF characteristics compared to the transistor in 4H-SiC technology.

TABLE II PROPERTIES OF MOSi$_{0.5}$Ge$_{0.5}$ AND MO(4H-SiC) TRANSISTORS.

Transistors / Parameters	**MOSi$_{0.5}$Ge$_{0.5}$**	**MOS(4H-SiC)**
I$_{Dsat}$(µA) (to V$_{GS}$=1.2V)	78.814	4.7449
V$_{th}$ (V)	0.3	≈1
I$_{ON}$/I$_{OFF}$ ratio	4,44 . 10^4	3,92 . 10^6
Operating temperature (°C)	200	≥ *550*
f_T (GHz)	22.975	9.8049
f_{MAX} *(MHz)*	18.4	0.22151

4. CONCLUSION

The electrical properties of MOSi$_{0.5}$Ge$_{0.5}$ and MO(4H-SiC) transistors in 130nm technology, with BSIM3v3 model, are investigated and compared using I-V and RC characteristics. This simulation was performed using PSpice software. We have shown that the parameters of Si$_{0.5}$Ge$_{0.5}$ and 4H-SiC semiconductors are responsible for the evolution of different electronic characteristics of our transistors. Our simulation shows that our MOSiC transistors operate correctly in a temperature range of -200°C to 200°C for MOSi$_{0.5}$Ge$_{0.5}$ and range of - 200°C to 600°C for MOS(4H-SiC) with 1.2V supply voltage. The studied transistors in Si$_{0.5}$Ge$_{0.5}$ and 4H-SiC technologies with

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BSIM3v3 model have yielded very satisfactory results.

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Authors Biography

Mourad Hebali: Laboratory, CaSiCCE, ENPO in Oran, B.P 1523 Oran El M'Naouar 31000 Algeria. Was born in Algeria in 1987, he received the M.S. degree in electronics from the ENP Oran, Algeria in 2014, he joined CaSiCCE laboratory as a PhD student, in 2015. His research interests include semiconductor physics (SiGe, SiC and GaAs), BSIM3v3 of temperature sensors, ISFET transistor for pH sensors, HEMT, SOI, DG-MOSFET, design and simulation of Micro and Nanoelectronics components and circuits, DRAM and SRAM memory cells.

Djilali Berbara: Laboratory, CaSiCCE, ENPO Algeria. Djilali BERBARA is a researcher in the laboratory characterization and simulation of electronic components and circuits and a PhD student in polytechnic national school ENPO. His research interests are: SiC and its applications in digital and analog circuits (Logic gates, DRAM, SRAM…). Temperature sensor.

Mohammed Benzohra: was born in Oran. He received the "Thèse d'Etat " degree in Electronic Engineering in 1980 from Paul Sabatier University, Toulouse, France. In 1981, he joined the Electronic Department of the "Université des Sciences et de la technologie d'Oran" in Algeria, working on defects in silicon devices. In 1995, he joined the LAAS du CNRS at Toulouse France working on ion implantation secondary-defect measurement for ULSI technologies. As professor at Rouen University since 1998, he is presently engaged in MEMS technologies and Polymer characterization.

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Djilali Chalabi: Laboratory, CaSiCCE , ENPO in Oran, B.P 1523 Oran El M'Naouar 31000 Algérie. **Prof D. Chalabi** was born in 1951 at M'hamid (Mascara) . He received the Radio Technician Diploma in 1971, an Engineer from degree USTOran in 1979, a Dr. Engineer from INPT Toulouse France in 1985 and a Ph.D. degree from USTOran in 2005. In 1979, he joined the department of Electrical and Electronic Engineering of ENSET Oran, as a lecturer and is now Professor of Analog and digital electronics. Current research interests include Bipolar, CMOS and BiCMOS transistors, design of analog and digital circuits, temperature sensors.

Abdelkader Saïdane: Laboratory, CaSiCCE , ENPO in Oran, B.P 1523 Oran El M'Naouar 31000 Algérie Prof. A Saïdane, was born in 1953 at Oued Sebbah, Algeria. He received the Diploma of Higher Studies (DES) in Solid State the University of Nottingham, UK, in 1981. He joined the department of Electrical Physics from the University of Oran, in 1976, and the PhD degree in Semiconductors from and Electronic Engineering of ENSET-Oran in 1981, as a lecturer and is now Professor of Semiconductor Physics. His research interests are Thermal Reliability of Devices and Systems, TLM Modeling and Novel Organic Solar Cells.

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