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Realization of MEMS Based Cantilever Structure Employing Simple Process Steps

Kamaljeet Singh
Sci/Engr, ISRO Satellite Center
Email: kamaljs@isac.gov.in

Ayyappankavu Venkateswaran Nirmal
Group Director, ISRO Satellite Center
Email: avnirmal@isac.gov.in

Abstract: *Cantilever is one of the basic structures in MEMS technology. It is a micro-beam which is hinged at one end. Compared to bridge structure the release of single supported structure is critical as stresses and structural stability plays an important role. The reliable release of the beam and its yield depends on the process steps which need to be simple and generic so that they are compatible with the standard foundries. Process integration and foundry limitations govern the choice of layers and release methodologies. Further the structures can be modified by doping to increase the sensitivity. This article will detail the process steps of creating the cantilever beam using bulk and surface micromachining process.*

Keyword: *MEMS; silicon; cantilever; micomachining;*

1. INTRODUCTION

Basic building blocks in MEMS are the cantilevers and bridge type microstructures. Singly supported beam i.e. cantilever is the basic structure in MEMS having wide range of applications encompassing Bio-MEMS, RF-MEMS, and Inertial MEMS even in AFM probe. Diaphragms and cantilevers beams are the basic type of suspended structure which are extensively employed for mechanical characterization also [1]. The realization of the free standing structures for these applications requires stress free membranes to realize straight beams. Normally the fixed-free type beam is having upward or downward bent due to residual stresses. The factors mostly responsible for this behavior are the process and design. The design part is fruitful only when the proper process steps are carefully chosen and incorporated by the designer at initial stages. Careful selections of process steps are utmost important for attaining higher yield of the realized structures.

The processes mostly adopted in MEMS structures are based on surface and bulk micromachining [2]. Surface micromachining devices are prone to stiction after sacrificial release which results in poor yield. Stiction free release depends on many factors and most important aspect is to achieve the process control. In turn, bulk micromachining is process intensive involving both front and back side operations which need to be chosen carefully so as to realize the reliable structures.

This article details the process steps for the realization of the cantilever structure utilizing bulk and surface micromachining process. The generic processes compatible to standard foundries are detailed providing step by step approach for the realization of reliable structures having better yield.

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2. MICROMACHININGTECHNIQUES

Micromachining techniques employed in the realization of the MEMS circuits are: bulk and surface micromachining [3].

TABLE1 COMPARATIVE MICROMACHINING PROCESS

Surface micromachining	Bulk micromachining
Single sided wafer operation	Both side wafer operation
Failures due to stiction, stresses	Rugged structures
Wider range of structural geometry	Limited range
Reduce sensitivity due to small mass/area ratio	Enhance sensitivity due to large mass/area ratio
Standard wafer	SOI, epi for precision
Smaller structures with better dimensional control	Bigger geometry

Table 1 shows comparative analyze of the machining processes. Standard material properties play an important role for realization of the cantilever structure [4]. Table 2 provides the comparative comparison

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of the material properties which are employed in design and realization of the structures.

TABLE 2 MATERIAL PROPERTIES

Material	Young's Modulus E (GPa)	Poisson's Ratio	Density, kg/m^3
Si_3N_4	222	0.27	2700
SiO_2	70	0.17	2510
Polysilicon	160	0.22	2230
Gold	78	0.44	19,300
Aluminium	70	0.35	2700

Mostly doped poly or aluminum layer are employed as structural layer (beam) which is anchored at the base. The process flow of the cantilever starts with the deposition of the oxide and nitride stack on top of the silicon wafer using the chemical vapor deposition (CVD) process.

2.1 Surface Micromachining

Surface micromachining process is based on the sacrificial layer release which is either oxide or polyimide as per foundry process. Surface micromachining process can be carried out using wet or dry etching process. It requires compatible structural materials, sacrificial materials and selection of proper etchants. The compatibility with the subsequent layers along with the faster etch rate is the criteria for selecting the structural layer. The masks generally employed for realization of the structures are: mesa, cantilever, implant, contact and metal and the major processes are Lithography, Chemical Vapor Deposition (CVD), Etching and Sputtering.

Process Flow for surface micromachining structures:

- Initial oxide nitride deposition. (Nitride at top and oxide at bottom) [CVD process]
- Oxide deposition /Polyimide. (Sacrificial layer deposition) [CVD/spin coating process]
- Oxide/polyimide patterning [Lithography]
- Nitride layer deposition (thickness to be optimized) [CVD process]
- Poly-silicon deposition (oxide layer can be put to compensate stresses)[CVD process]
- Piezo implant [Implantation process]
- Isolation Nitride Deposition [CVD process]
- Contact Etch[Lithography/Etching]
- Metal Layer Deposition[Sputtering]
- Metal Etch[Lithography/Etching]
- Sacrificial layer etching (wet/dry)

The selection of etchant material requires higher etch selectivity whereas selection of structural material is governed by high fracture strength, good wear resistance and low residual stress. Piezo implant steps increases the sensitivity of the structures whereas layer of poly is sandwiched in-between oxide so as to compensate the stresses.

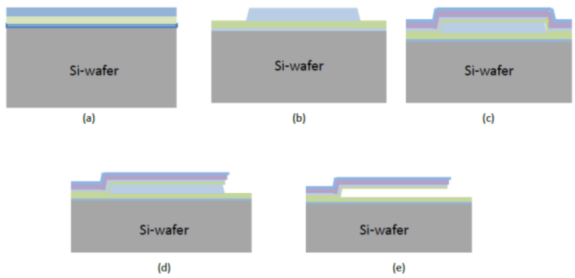

Figure 1 Process steps related with surface micromachined cantilever

The beam having 1-2 um air gap can be achieved and subsequent process can be tweaked such as bottom layer of aluminum can be introduced as per application requirements such as RF-MEMS switch.

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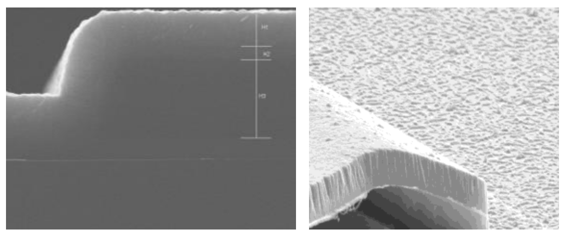

Figure 2 SEM view of the unreleased surface micromachined cantilever and view of a released structure

The SEM pictures of the structure having various layers are shown in Figure2. The release methodology can be ashing (polyimide), wet (HF based for oxide), CPD or XeF_2 [4]. The reliable release of these structures depends on the process parameter, design and techniques. Stiction is one of the failure mechanism mostly encountered in the cantilever structures and various methodologies such as bumps, creating hydrophobic surface in addition to releasing structural layer at the end of the wet processes can overcome it. The main issue in processing of the structures depends

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on the choice of structural and sacrificial layer [5] and tentative list is shown in Table 3.

TABLE 3 TENTATIVE LIST OF STRUCTURAL AND SACRIFICIAL MATERIAL

Sacrificial Layer	Structural Layer	Removal methodology
Phospo silicate glass (PSG) oxide	Poly-Si	HF
Polyimide	Al/Poly-Si	Ashing
Poly-Si	SiN	TMAH

As the sheet resistance for aluminum is 200 times better than poly layer so aluminium layer is preferred compared to doped poly

2.2 Bulk Micromachining

Bulk micromachining process is based on the processing of wafer from both the sides. The etch depth is controlled either by the {111} plane, time controlled etching, etch stop due to insulator layer of SOI or by using electrochemical etch stop technique. Highly doped silicon exhibits (> $1x10^{19}cm^{-3}$) negligible etch rate in wet anisotropic etchants. In case of SOI, uniform thickness can be achieved without creating contamination or residual stress which otherwise is associated with other techniques.

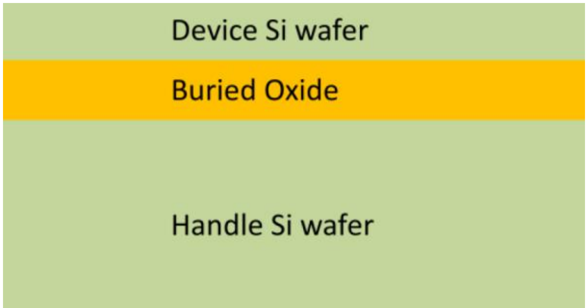

Figure 3 Cross section view of the SOI wafer [6]

Process Flow for bulk micromachining structures:

Bulk micromachining process uses various etchants such as ethylenediamine pyroatechol (EDP), potassium hydroxide (KOH) and tetramethyl ammonium hydroxide (TMAH) The etching in silicon is dependent on the crystallographic orientation resulting from isotropic or anisotropic etching. Silicon etches out isotropically in all directions independently using wet methodology and is dependent on time, temperature and etchant concentration. HNA solution yield isotropic etching in silicon whereas anisotropic wet etchants for micromachining are KOH, EDP, TMAH, Hydrazine where TMAH ($(CH_3)_4NOH$) is generally employed due to CMOS compatibility as alkali metal ions are detrimental to CMOS structures. Conventional alkali metal hydroxide (KOH) etching provides well-defined pattern but possibility of pyramidal hillock on the etched surface exists and possibility of hole formation on etched membrane in case of hydrazine is observed. Ethylenediamine-pyrocatechol (EDP) and Hydrazine solutions are carcinogenic and toxic. EDP and TMAH chemicals are having minimal effect on oxide layer along with providing smooth surface but having slower etch rate. The various steps taken for bulk micromachining are:

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1. Screen Oxidation [CVD process]
2. Substrate mask and etching[Lithography]
3. Implant 4E15, 30KeV [Implantation]
4. CVD Oxide deposition-(Part-1)
5. Oxide etching [Etching]
6. CVD Oxide deposition-(Part-2)
7. Contact etch [Lithography/Dry Etching]
8. Metal deposition [Sputtering]
9. Metal etching[Dry etching]
10. CVD Oxide 2 Etch (S.No6)
11. Backside Oxide stripping[Etching]
12. Backside thick oxide deposition [CVD]
13. Front side silicon etch [Etching]
14. Back side silicon etch
15. SOI layer removal

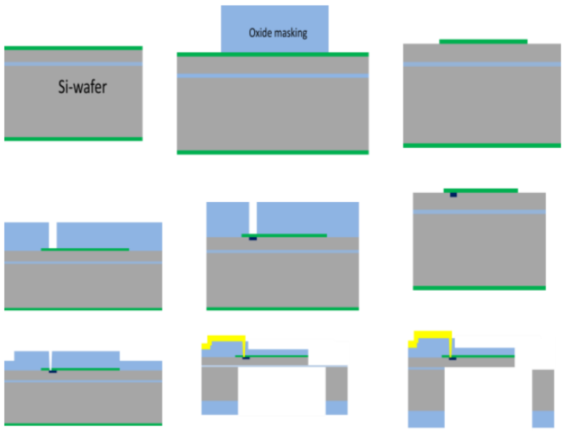

Figure 4 Process steps related with bulk micro-machined cantilever (L-R)

Various masks such as implant, contact, metal and cavity are employed to realize the structures. The wet etching is crystallographic dependent and primarily <100> oriented silicon wafer is taken for the processes [6]. Both the processes are intiated with cleaning using RCA1[H_2O:NH_4OH:H_2O] and RCA-2 [H_2O:HCl:H_2O_2].

Both wet and dry process can be employed for the realization of bulk micro-machined based cantilever.

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Wet process is faster but due to anisotropic etching the controlling of the exact depth is difficult is difficult and can be easily overcome by employing SOI wafer [7]. The etched roughness strongly depends on the crystallographic orientation.

3. CONCLUSION

Fabrication steps for the realization of cantilever structure employing simple process steps are presented. The realization of the same demands careful process selection along with higher yield. The advantage of the surface micromachining process is the independence from employing special process or wafer compared to bulk micromachining process. It is recommended to fabricate test structures such as spiral, stress vernier, resonator, guckel etc for stabilization of various process parameters. MEMS based cantilevers are most popular in disease detection, energy harvesting devices, accelerometers and current sensors. The simple process steps using both bulk and surface micromachining presented can yield the realizable devices and will be useful for researchers to realize the devices with faster turnaround time.

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REFERENCES

[1] Micro and Smart Systems, G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat and V.K. Aatre ,Wiley India,2011

[2] Prem Pal & Kazuosato,Silicon Wet Bulk Micromachining for MEMS, Pan Stanford Publishing Pte Ltd,2017

[3] Kamaljeet Singh, A V Nirmal," Reliability Aspects in RF-MEMS Circuits for Space Applications,"Journal of Engineering and Technology,4(6),pp 1-11,2016

[4] C R M Grovenor, Microelectronic material, IOP Publishing Ltd,1989

[5] James M Bustilo,R T Howe,R S Muller," Surface Micrtomachining for Microelectromechanical Systems," Proccedings of the IEEE,Vol 86,No 8,August 1998,pp 1552-1574

[6] S.Udara,P H S Tejo Murthy," Fabrication and characterization of MEMS/NEMS based piezoresistive cantilever for the detection of change in resistance with time at different experimental conditions using OmniCant,"Materuials Today:proceedings (ICNANO-2016) 4(2017),12261-12270

[7] Kamaljeet Singh, A V Nirmal, "Silicon Wafer Specifications and Its Selection Criteria", International Journal of Advances in Computer and Electronics Engineering, Volume 3, Issue 5, May 2018, pp. 9–13

Authors Biography

Kamaljeet Singh has obtained M. Tech (Microwaves) from Delhi University in 1999 and awarded PhD in 2010. He joined ISRO Satellite center, Bangalore in 1999 where he worked in GEO-receiver. From August 2006 – Feb 2016 he was posted in Semi- Conductor Laboratory, Chandigarh and worked in the areas of RF-MEMS and sensors. He is presently working in SEG group at ISAC.

A V Nirmal obtained his B.E in Mechanical Engineering from Kerala University in 1984. He joined VSSC, Trivandrum in 1984 and has been working in ISAC since 2004. He is credited with productionzation and delivering of all sub-systems of IRS and Geosat missions. He was involved in the design and development of various mechanical systems for both Launch vehicle and satellites and establishment of test facilities. He is presently working as Group Director, Systems Engineering Group, ISRO Satellite Centre

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