www.ijaceeonline.com ISSN: 2456 - 3935

International Journal of Advances in Computer and Electronics Engineering
Volume 3, Issue 6, June 2018, pp. 6–12

Symmetric Stacking Counter Based Testing

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Abstract: *Parallel counters are enter components in numerous number juggling circuits, particularly quick multipliers. Another paired counter plan is proposed. It utilizes Multiplexer (MUX) based full adder circuit, which aggregate the greater part of the "1" bits together. In proposed structure one xor obstruct in traditional snake is supplanted by multiplexer square with the goal that the basic way delay is limited. Counter-based systems have been proposed for use in worked in test set installing. A solitary counter or various counters might be utilized with one or different seeds. This paper concentrates on region productive blame tolerant full snake outline. This outline can repair single and twofold blame without intruding on the typical operation of a framework. A framework must be blame tolerant to diminish the disappointment rate in the blame area. In this approach self-checking full snake is utilized recognizing the blame in light of inside usefulness. The idea of self-checking and blame tolerant is acquainted with manage the issue of blame. Subsequently the operations associated with the proposed configuration is performed utilizing self-checking and mistake rectifying counter based full snake plan. Moreover, counters might be joined with Read Only Memory (ROM) proposed framework coded in Verilog Hardware Description language (VHD) and mimicked utilizing Xilinx 12.1.*

Keyword: *Multiplexer, Counter, Full adder, Fault tolerant, stacking, Read Only Memory (ROM);*

1. INTRODUCTION

A (n, m) parallel counter is a circuit which gives a m-bit tally of the quantity of the n-inputs that are rationale ONES. A counter contrasts from a compressor in that compressors have convey information sources and convey yields notwithstanding the "typical" data sources and yields, while counters don't have convey information sources and yields. The most broadly utilized parallel counters are full adders which are (3:2) counters and half adders which are (2:2) counters.

Bigger parallel counters are particularly helpful in the execution of generally utilized flag handling components, for example, multipliers, assembles, and so on. The speed of multipliers is a basic issue in deciding the execution of chip whatever is left of this concise presents the counters in area I. Next the related works and quick double counter utilizing symmetrical stack are considered in Area II. At that point, in Segment III, the proposed is displayed. Segment IV shows an exploratory Outcomes and execution investigation to outline the adequacy of the equipment security approach. At long last, the conclusions are abridged in Segment V.

In this paper [1] segment pressure multiplier to outline a strategy for section limited by the compressor based multipliers. So the principle downside is the higher equipment multifaceted nature. Be that as it may, the Energy Delay Product (EDP) is marginally higher than the lower arranging compressors. Wallace Tree multiplier utilizing fast counter to be intended for the counter approach. This compressor utilizes counter property. With the goal that the yield of compressor gives number of 1's at input. So the principle disadvantage for defer overhead [2].

In the novel models took after by the Wallace Tree multiplier circuit. In this manner the effective (m,n) parallel counters are the fundamental mux counter then the mux based approach includes extra of the complex [3]. Bolster forward and criticism interconnections are inferred by the techniques utilized as a part of the aloofness for the interconnected in the symmetrically disseminated framework. Along these lines the encourage forward techniques to be held at the steering multifaceted nature [4].

In the fast increase of 8-4 and 9-4 compressors utilizing the higher request of the compressor can be adequately utilized for rapid duplications. Subse-

Cite this paper:

Duraipandi Ajitha, J. Mangaiyarkarasi, "Symmetric Stacking Counter Based Testing", International Journal of Advances in Computer and Electronics Engineering, Vol. 3, No. 6, pp. 6-12, June 2018.

ISSN: 2456 - 3935
International Journal of Advances in Computer and Electronics Engineering
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quently the augmentation is a crucial operation in the vast majority of the flag handling calculation [5]. In this paper took after by the fast operations of the full viper based counter. Along these lines the counter to be examined by the engineering of the Wallace multipliers. So the fundamental disadvantage for this paper utilizing high power utilization [6]. In the quick number juggling circuits utilizing low power, low voltage (5:2) compressors cell. At that point the compressor cell is as needs be performed by low power compressors. In such manner numerous inventive outlines for essential rationale capacities utilizing pass transistors and transmission doors have showed up in the writing as of late. This may likewise brings about problematic operations as the power supply voltage is downsized. Subsequently the 16 transistor included cell (16T) given isn't a decent decision for low voltage operations [7].

The piece of discovery and gathering techniques utilizing multi-scale symmetric. It's recuperating and gathering symmetric parts [8]. In this paper to outline a proficient reversible multiplier utilizing leather treated Energy Delay Adder (EDA). In this way the strategy can be executed as low power planning by reversible rationale entryways. So it can be possess the substantial information, yield necessities [9]. Feed forward and feedback interconnections are derived by the methods used in the passivity for the interconnected in the symmetrically distributed system. Accordingly the encourage forward techniques to be held at the steering multifaceted nature [4]. In the rapid duplication of 8-4 and 9-4 compressors utilizing the higher request of the compressor can be adequately utilized for fast augmentations. Thus the multiplication is a fundamental operation in most of the signal processing algorithm [5]. In this paper followed by the high speed operations of the full adder based counter.

Thus the counter to be analyzed by the architecture of the Wallace multipliers. So the main drawback for this paper using high power consumption [6]. In the fast arithmetic circuits using low power, low voltage (5:2) compressors cell. Then the compressor cell is accordingly performed by low power compressors. In this regard many innovative designs for basic logic functions using pass transistors and transmission gates have appeared in the literature recently. This may also results in unreliable operations as the power supply voltage is scaled down. Hence the 16 transistor added cell (16T) given is not a good choice for low voltage operations [7].

The part of detection and grouping methods using multi-scale symmetric. It's recovering and grouping symmetric parts [8]. In this paper to design a efficient reversible multiplier using tanner EDA. Thus the method can be performed as low power designing by reversible logic gates. So it can be occupy the large input, output requirements [9].

In this paper, an advanced configuration for a symmetric multilevel voltage source inverter is proposed [10]. The proposed inverter is able to generate the nine levels using a lower number of circuit devices including power semiconductor switches. Moreover, the reduced amount of on-state switches in the suggested configuration decreases voltage drops. Power losses are diminished, the given simulation results confirm the feasibility of the proposed configuration. To approve the practicability of the proposed inverter, a prototype of the proposed topology has been implemented [11]. Finally, simulation results show that the obtained results are in good agreement. As a result, the total cost is considerably reduced, and the control scheme gets simpler.

In this work, changing the internal equations yields a new realization with a 6 XOR delay. In another structure has been disclosed, the critical path delay of which equals 7XORs. As seen, the counters in each gray polygon build a 4:2 compressor. Comparing the proposed implementation [12] with this architecture indicates that our implementation has less interconnections and XOR delays. It moreover reduces the number of stages required for eliminating carry propagation delay from 3 stages to 2.

This work presents a 1.2-ns16×16-Bit Binary Multiplier Using High Speed Compressors [13]. For higher request duplications, an enormous number of adders or compressors are to be utilized to play out the incomplete item expansion. We have lessened the quantity of adders by presenting exceptional sort of adders that are skilled to include five/six/seven bits for each decade. These adders are called compressors.

Twofold counter property has been converged with the compressor property to grow high request compressors. Employments of these compressors allow the decrease of the vertical basic ways. A 16×16 piece multiplier has been produced utilizing these compressors. These compressors make the multipliers quicker when contrasted with the ordinary outline that have been utilized 4-2 compressors and 3-2 compressors.

New implementation for 7:2 compressors, based on the conventional architecture, is proposed. According to the results, the design presented achieves a remarkable improvement in terms of speed (especially in low voltages) and power consumption over the best counterpart [14].

By using the conventional 7:2 architecture as basis and changing its internal equations as follows, our proposed implementation (Figure 4) could achieve a better performance. In our novelty the critical path delay equals 6 XORs, which means the overall delay is reduced by one XOR as compared to the conventional counterpart. Applying the following changes to the above equations reduces the relation between the sum and carry generating trees and thus causes.

This paper proposes various designs for the counter based Wallace multipliers to investigate their exe-

ISSN: 2456 - 3935
International Journal of Advances in Computer and Electronics Engineering
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cution for different piece lengths. Plans are blended utilizing Synopsys Design Compiler in 90 nm process innovation and the post union deferral and power comes about are gotten by utilizing Synopsys Prime Time [15]. The proposed counter based Wallace multipliers are likewise contrasted with conventional Wallace multiplier with assess the vitality per task of the two plans. The combination comes about demonstrates that the Power-Delay Product of the counter based Wallace multiplier is up to 17% lower when contrasted with the customary Wallace multiplier.

This paper [16] presents a Low-voltage low-control CMOS full stack. Low power plan of VLSI circuits has been distinguished as a basic innovative need lately because of the popularity for versatile shopper gadgets items. In such manner numerous creative outlines for essential rationale capacities utilizing pass transistors and transmission doors have showed up in the writing as of late. These plans depended on the instinct and astuteness of the fashioners, without including formal outline methodology.

2. COUNTER IMPLEMENTATION

Much of the time, the outline of (7:3) parallel counter is appeared. By and large such counters are sufficiently expansive to outline the ideas without getting hindered with an excessive amount of detail. Now and again, counters of different sizes are appeared to show the technique.

The limit entryway counters multipliers incorporated a plan for a (7:3) counter executed with transforming edge doors gives a meaning of upsetting edge entryways. There are n twofold data sources, each with a comparing weight. On the off chance that the total of the weights of the information sources that are rationale ONES surpasses the edge of the entryway the yield is a rationale ZERO, generally the yield a rationale ONE. At that point the acknowledgment of a (7:3) parallel counter with three reversing limit doors.

This circuit utilizes three limit doors with seven, eight and nine information sources and edges of four, six and seven, separately. The postponement of the slightest huge piece of the tally, y_2, is three door delays, the deferral of the center piece, y_1, is two entryway delays, and the deferral of the most huge piece, y_0, is one entryway delay. This approach has not been generally utilized, maybe due to the trouble of acknowledging huge edge doors with exact limits.

This counter in view of an exchanging tree actualized with transfers expressed to be an expansion of a thought that is because of Falk off. The main counter information controls a solitary shaft twofold toss transfer, the second info controls a twofold post twofold toss hand-off, the third information controls a triple post triple toss hand-off, and so forth. The intricacy of this approach develops as the square of the quantity of sources of info, making the cost restrictive for the acknowledgment of huge counters.

The hand-off switches can be actualized with superconducting cryotrons. In VLSI, CMOS domino rationale is additionally reasonable for the acknowledgment of exchanging tree. Exchanging trees for the three bits of a (7:3) parallel counter. The acknowledgment of the exchanging trees with domino rationale. Albeit customary outline tenets would not permit the same number of levels of transistors between the V_{dd} and V_{ss} supplies as the eight levels of this circuit, reenactments demonstrate that execution of the structure does not endure.

Cultivate and Stockton built up a counter actualized with full and half adders. This techniques (31:5) parallel counter which comprises of collection the counter contributions to [n/3] sets of three lines every which are contribution to full adders (where: [x] signifies the biggest whole number not exactly or equivalent to x). The [n/3] whole and [n/3] convey yields of the full adders (and any natural contributions to the counter) are assembled into threes and connected to second (littler) arrangements of full adders, and so on. The quantity of full adders to understand a (n, m) parallel counter is inferred as not exactly or equivalent to n.

The deferral for the slightest critical piece of the tally is m – 1 full snake delays (accepting that the postponement from any contribution to any yield of a full viper is 1 full snake delay) and the deferral for the most noteworthy piece of the check is 2m – 3 full viper delays. It is shown that the parallel adders can then again be acknowledged with quick adders. It was recommended that read no one but recollections could be utilized; yet convey look ahead adders or contingent whole adders would be a more proper decision with current innovation. In the event that the parallel viper has postpone practically identical to a full snake delay, this approach gives all bits of a (n, m) parallel counter in m – 1 full snake delays.

3. SOLUTION METHODOLOGY

A double counter plan is proposed. It utilizes 3-bit stacking circuits, which assemble the greater part of the "1" bits together, trailed by a novel symmetric technique to consolidate sets of 3-bit stacks into 6-bit stacks. The bit stacks are then changed over to paired checks, creating 6:3 counter circuits with no xor entryways on the basic way. This shirking of xor doors brings about quicker outlines with productive power and territory use.

In VLSI reenactments, the proposed counters are speedier than existing parallel counters and furthermore devour less power than other higher request counters. Furthermore, utilizing the proposed counters in existing counter-based Wallace tree multiplier models decreases inertness and power utilization.

Figure.1 shows the fundamental full stack circuit. It can be utilized ordinary counter for the plan. They are

ISSN: 2456 - 3935
International Journal of Advances in Computer and Electronics Engineering
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having XOR-XNOR for the info X1, X2 and X3 is associated by the immediate contribution for mux.

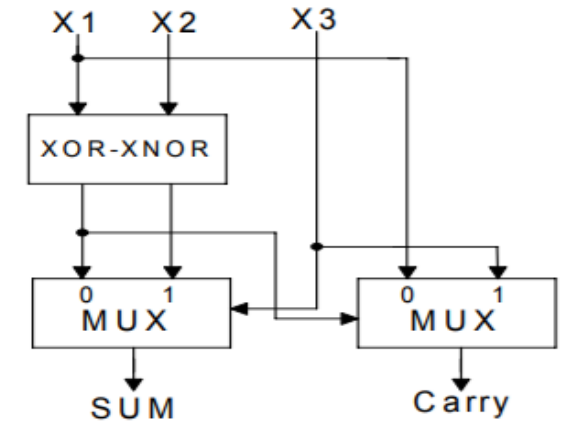

Figure 1 Conventional counter

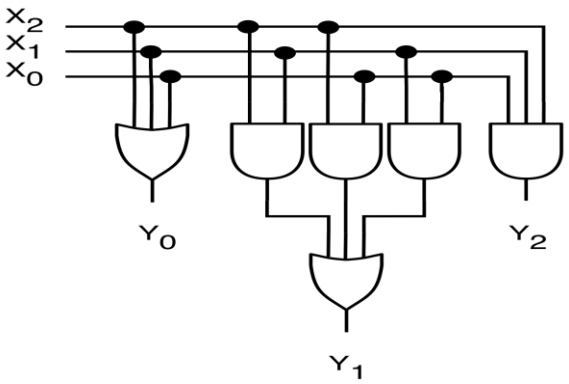

Figure 2 Three-bit stacker circuit

The Figure 2 shows the ordinary counter outlines gives from total and convey yield. given sources of info X_0, X_1, and X_2, a 3-bit stacker circuit will have three yields Y_0, Y_1, and Y_2 to such an extent that the quantity of "1" bits in the yields is the same as the quantity of "1" bits in the information sources, yet the "1" bits are assembled together to one side took after by the "0" bits. Unmistakably the yields are then shaped by,

$$Y_0 = X_0 + X_1 + X_2$$
$$Y_1 = X_0X_1 + X_0X_2 + X_1X_2$$
$$Y_2 = X_0X_1X_2.$$

Specifically, the main yield will be "1" if any of the sources of info is one, the second yield will be "1" if any two of the information sources are one, and the last yield will be one if every one of the three of the data sources are "1." The Y_1 yield is a lion's share work and can be executed utilizing one complex CMOS door. Figure 3 shows the symmetric stacking technique can be utilized to make a 7:3counter too. The 7:3 counters are alluring as they give a higher pressure proportion. The plan of the 7:3 counter includes figuring yields for C1 and C2 accepting both X6 = 0 (which coordinates the 6:3 counter) and expecting X6 = 1. We figure the S yield by including one extra XOR door

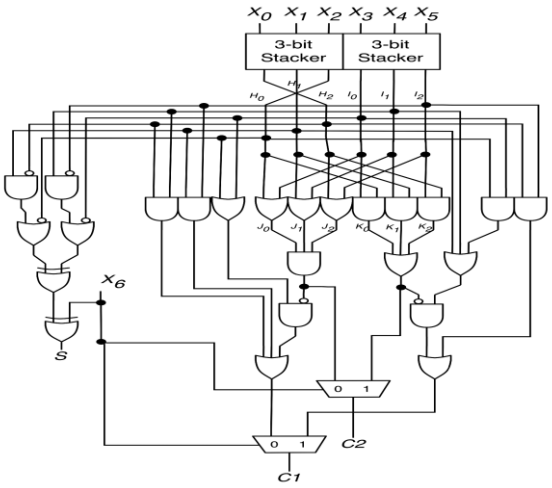

Figure 3 7:3 Counters based on symmetric stacking

Essential full adder circuit. It can be utilized traditional counter for the plan. They are having XOR-XNOR for the information X1, X2 and X3 is associated by the immediate contribution for mux. The customary counter outlines gives from whole and convey yield.

The proposed changed full stack circuit as appeared in Figure 4. It comprises of two 2:1 MUX and a XOR entryway. In the proposed structure, one XOR obstruct in the regular full viper is supplanted by a multiplexer square with the goal that the basic way delay is limited. As can be seen, the basic way delays.
(i.e.) delay= XOR + MUX

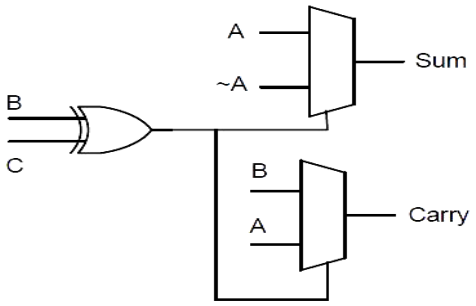

Figure 4 Proposed Full Adders

The Proposed full adders of the other two data sources are given to XOR entryway, the yield of which will go about as a select line to both the multiplexers. The contributions of the second multiplexer are, the bits other than the convey bit. This special

ISSN: 2456 - 3935
International Journal of Advances in Computer and Electronics Engineering
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method for outlining prompts the lessening of the exchanging movement, which thus diminishes the power. What's more, the basic way delay is likewise decreased contrasted with the current outlines examined in writing, which prompts diminishment in deferral and hence expanding the speed. Operation of the proposed full snake can be clarified as takes after:

a) When both B and C are zero or one, sum = A;
b) When either of B or C is one and another is zero, sum=A;
c) When both B and C are zero or one, carry= B; When either of B or C is one and another is zero, carry=A;

This can be implemented by using second MUX with XOR output as selection line. Since XOR employs most of the power consumption in the adder circuit, by reducing number of XOR gates, power consumption of the full adder can be reduced. The proposed full adder is applied into array multiplier reduction stage to validate the effectiveness. In array structure the partial products is divided into certain levels. In each level, whenever there are three bits, full adder has to be used. Out of the three inputs, one input and its complement is provided as inputs to the first multiplexer.

4. RESULTS AND DISCUSSION

The Figure 5 demonstrates the results for simulation of proposed full adder network.

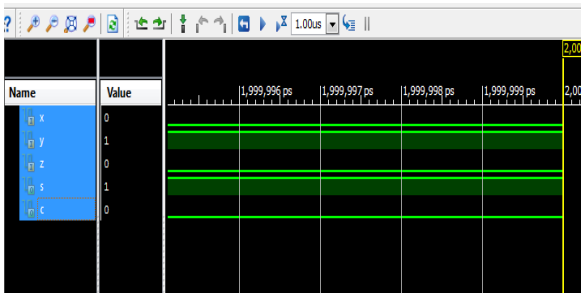

Figure 5 Simulation Result for Proposed Full Adders

The Figure 6 demonstrates that plan outline of the proposed framework. It gives the assessed estimations of the capacity.

Figure 7 shows the Power examination of proposed framework is appeared in above fig 7. This investigation mostly focused on the number IOs in the whole framework to acquire the yield. In the whole framework, the accessible quantities of IOs are 12.0 and the IOs used to get the yield are 0.008. The aggregate accessible power in the framework is 0.081 W and thus the use of energy is 0.2 W.

Figure 8. shows the Power New Full Adder (NFA) Counters the proposed has been reenacted and the union report can be acquired by utilizing Xilinx ISE 12.1i.

The Figure 9 given underneath is demonstrated that there is a significant lessening in time and zone in view of the execution comes about which have been finished by utilizing Simple 3 processor. The proposed calculation altogether lessens zone utilization when contrasted with the current framework.

Target Device:	xc3s100e-5vq100	•Errors:	No Errors
Product Version:	ISE 12.1	•Warnings:	4 Warnings
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	4	960	
Number of 4 input LUTs	8	1920	
Number of bonded IOBs	10	66	

Detailed Reports				
Report Name	Status	Generated	Errors	Warnings
Synthesis Report	Current	Fri Sep 22 09:28:57 2017	0	4 Warnings (4 new)
Translation Report	Out of Date	Thu Sep 14 12:35:15 2017		
Map Report	Out of Date	Thu Sep 14 12:35:29 2017		
Place and Route Report	Out of Date	Thu Sep 14 12:35:54 2017		

Figure 6 Design Summary of .New Full Adder (NFA) Counters

The different parameters utilized for figuring existing and proposed frameworks with Austere 3 processor are given in the Table.1

TABLE.1 COMPARISON OF EXISTING AND PROPOSED SYSTEM

S.NO	Parameter	Existing	Proposed
1	Slice	9	4
2	LUT	15	8

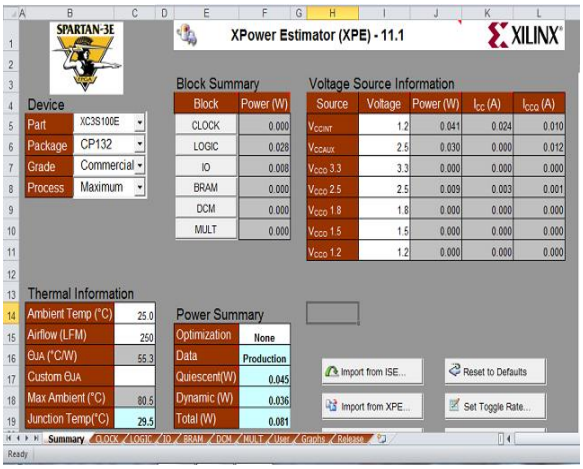

Figure 7 Power Analysis New Full Adder (NFA) Counters of System

ISSN: 2456 - 3935
International Journal of Advances in Computer and Electronics Engineering
Volume 3, Issue 6, June 2018, pp. 6–12

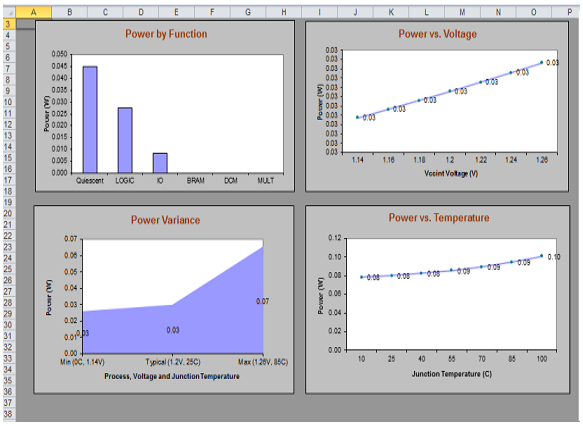

Figure 8 Power New Full Adder (NFA) Counters

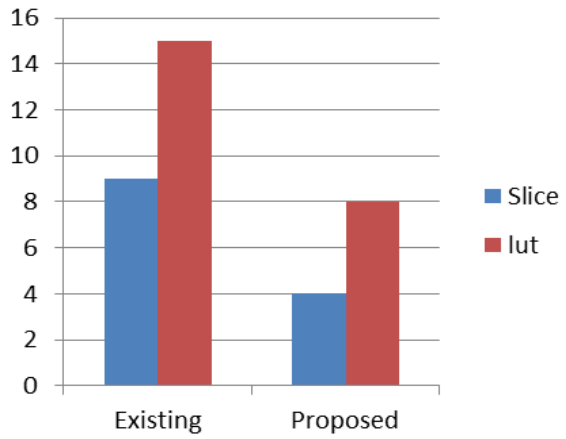

Figure 9 Performance Analysis

5. CONCLUSION

In this paper, a plan strategy for region viable and speed effective counter is planned and reproduced. A twofold counter in view of a novel symmetric piece Aggregate and convey computation approach is proposed. We demonstrated that this tallying strategy can be utilized to actualize 6:3 and 7:3 counters, which can be utilized as a part of any parallel multiplier circuit to include the fractional items. We showed that 6:3 counters actualized with this NFA system accomplish higher speed than other higher request counter outlines while diminishing force utilization.

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ISSN: 2456 - 3935
International Journal of Advances in Computer and Electronics Engineering
Volume 3, Issue 6, June 2018, pp. 6–12

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Cite this paper:

Duraipandi Ajitha, J. Mangaiyarkarasi, "Symmetric Stacking Counter Based Testing", International Journal of Advances in Computer and Electronics Engineering, Vol. 3, No. 6, pp. 6-12, June 2018.